(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 593 012 A2

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: 93116496.6

(22) Date of filing: 12.10.93

(51) Int. Cl.5: G09G 1/16, G06F 3/14

(30) Priority: 13.10.92 JP 274035/92

(43) Date of publication of application:
20.04.94 Bulletin 94/16

(84) Designated Contracting States:
DE GB

(71) Applicant: HITACHI, LTD.
6, Kanda Surugadai 4-chome
Chiyoda-ku, Tokyo 100(JP)

(72) Inventor: Kohiyama, Tomohisa
Manshon Akaseki 305,
523, Kamikashiocho
Totsuka-ku, Yokohama-shi(JP)
Inventor: Yamagishi, Masami
Hitachi Zamaryo 314,
5816-2, Iriya-3-chome
Zama-shi(JP)
Inventor: Yamada, Takahiro
241-180, Fukayacho,
Totsuka-ku
Yokohama-shi(JP)
Inventor: Kamo, Munekazu
22-10, Shibusawa-2-chome
Hadano-shi(JP)
Inventor: Nomi, Makoto
Tsukubadai Terasu 103,
663, Ichige
Katsuta-shi(JP)
Inventor: Iwai, Noriyuki, Hitachi
Utsukushigaokaryo W232
40-1, Utsukushigaokanishi-2-chome
Midori-ku, Yokohama-shi(JP)
Inventor: Minobe, Randy
4125 Cranford Circle
San Jose, Ca 95124(US)
Inventor: Jenney, Kim
1120 Morse St.
San Jose, Ca 95126(US)

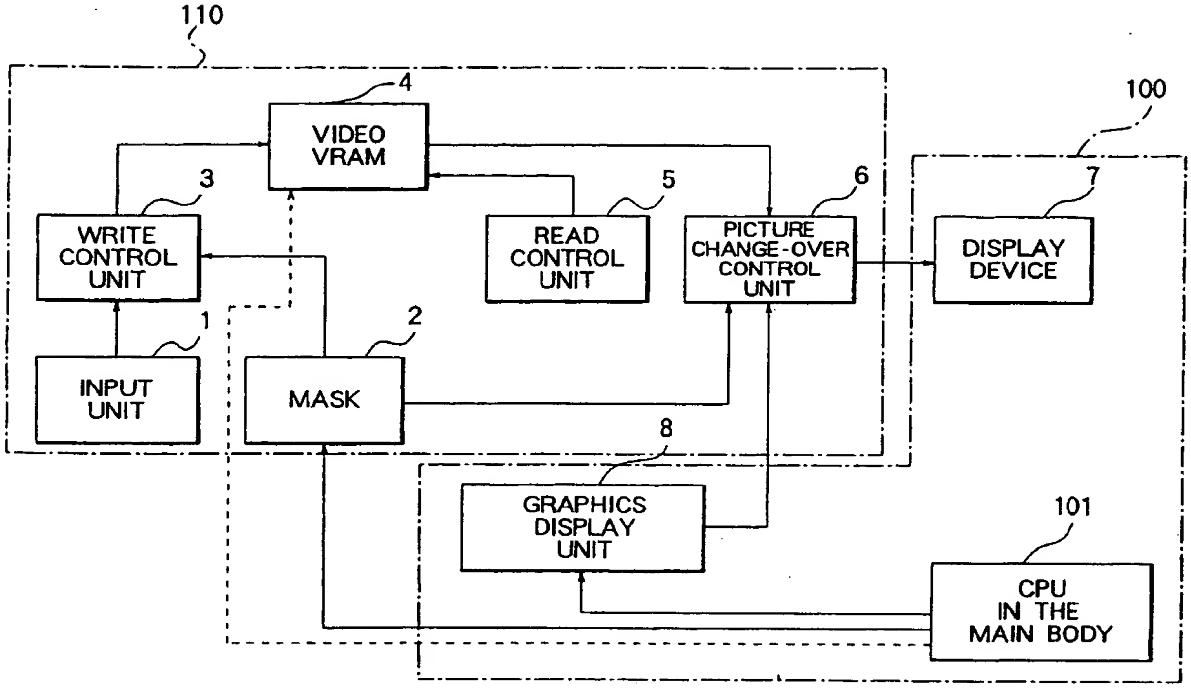
(74) Representative: Altenburg, Udo, Dipl.-Phys. et al
Patent- und Rechtsanwälte,
Bardehle . Pagenberg . Dost . Altenburg .
Frohwitter . Geissler & Partner,
Galileiplatz 1
D-81679 München (DE)

(54) **Video picture display device and method for controlling video picture display.**

(57) A video picture written in the bit map memory (4) is displayed in a redetermined area on the display screen (70) of the display device (7) within the computer main body (100). The masking memory (2) having a bit number equal to or less than the number of the pixels of the video picture to be inputted is provided separate from the bit map memory (4). When the pixel data of the video picture data has been inputted, the input pixel data is selectively written in the bit map memory (4) based on the contents of the masking memory (2). In displaying a compressed picture of the input video picture on the display screen, an oblique line generating algorithm is used.

EP 0 593 012 A2

FIG. 1


110
100
4
VIDEO VRAM
3
WRITE CONTROL UNIT
5
READ CONTROL UNIT
6
PICTURE CHANGE-OVER CONTROL UNIT
7
DISPLAY DEVICE
1
INPUT UNIT
2
MASK
8
GRAPHICS DISPLAY UNIT
101
CPU IN THE MAIN BODY

BACKGROUND OF THE INVENTION

The present invention relates to a picture display device known as a scan converter, and relates more particularly to a video picture display device which is suitable for displaying an inputted video picture on a display screen of a computer equipped with a window environment.

The scan rate of a display screen of a personal computer (hereinafter to be abbreviated as a "PC") or a work station (hereinafter to be abbreviated as a "WS") which is used as a computer is generally different from that of a screen of a television set or the like. Therefore, a video picture display device for displaying a video picture on the display screen of the PC or the WS by combining video pictures of a television set or the like requires a change of the scan rate. Accordingly, the video picture display device is also called a scan converter.

Normally, the scan converter stores data of a video signal in a video memory which is a memory unit (also called a frame memory). In the present specification, the scan converter will hereinafter be called a "video VRAM (video random access memory)" in order to distinguish between this memory unit and a video memory for graphics which is located in the computer such as a PC and a WS. A read control unit within the scan converter (a graphics display unit) reads data within the video VRAM to match a display timing signal at the computer side and a picture change over control unit suitably changes over between read data from the video VRAM and read data for graphics display at the computer side and send the data to the display device. Thus, video pictures of the television or the like are combined for display on the display screen of the computer. Generally, a CRT display or a liquid crystal panel is used as a display device of the computer such as a PC or a WS.

In recent years, great importance has come to be attached to an application for monitoring a television broadcasting program or for displaying a motion picture or a still picture such as animation pictures, for example, on the display device of the computer. An application for displaying various kinds of pictures as described above will be called a multi-media application in the present specification.

In the mean time, along with the improvement in the performance of a processor for controlling a computer system as a whole and an increase in the capacity of the main memory loaded in the computer, a system environment as represented by a window system (hereinafter to be referred to as a "window environment") has come to be employed extensively in recent years. Under this window environment, a user opens (or displays) at least one square window called a window on the screen of the display device to have a display of a desired application program within each window.

Based on the window environment, a plurality of video pictures can be displayed simultaneously on a single screen so that this window environment can be combined with a multi-media application in a very suitable manner. Since the user can open a plurality of windows at desired positions on the screen of the display device under the window environment, there is a case, however, that the windows may be superimposed with each other. For example, when two windows are partly superimposed, the rear side window portion which is hidden by the front window needs to be controlled not to be displayed.

When a multi-media application has been operated in the window environment, there arises such a case that a video picture is displayed within a window at the rear side of a plurality of windows which are partly superimposed with each other so that a part of the video picture can not be displayed. Since the video picture data is being stored within the video VRAM which is separate from the graphics video memory, as mentioned above, it is necessary to have some skill to read video picture data in order to make a display of the video picture (particularly a motion picture) that has such an undisplayed portion as described above.

Broadly, two methods are known as methods for obtaining a video picture which has a partly hidden portion.

One method is to control so that writing of a partly hidden portion is prohibited when video picture data is to be written in the video VRAM. This method will be called a writing mask control system in the present specification.

The other method is to control, at the time of reading video picture data from the video VRAM, so as to select which one of video picture data that has been read from the video VRAM and graphics data that has been read from the graphics video memory should be displayed. This method will be called a keying control system in the present specification.

A conventional writing mask control system is disclosed in the "Nikkei Electronics", June 24, 1991 issue (No. 530), pp. 165-176. In the above literature, a 16-plane video memory is disclosed which combines the graphics video memory and the video VRAM into one. One of the 16 planes is used as a writing mask plane for video picture data and the remaining 15 planes are allocated to either the video VRAM or the graphics video memory.

Based on this structure, before writing video picture data into the planes that have been allocated to the video VRAM, it is necessary to read mask data of the mask plane and check for each

dot data of the video picture to see whether the corresponding dot data is writable or write prohibited in the video VRAM planes. If the mask data that has been read shows a write permit, the corresponding dot data is written in the video VRAM planes, and otherwise the data is abandoned.

Under the above-described structure, the writing mask data is necessary by the number equivalent to that of the pixels that constitute the display screen of the computer display device. For example, when the display screen of the display device is structured by the pixels of 1280 x 1024, minimum 1280 x 1024 x 1 bits are necessary and since the mask plane is structured by combining a plurality of general semiconductor memory devices, 2048 x 1024 x 1 bits are necessary in total. This corresponds to two semiconductor memory devices of one megabits.

On the other hand, in the case of a video signal of a television set, it is general that the video signal is digitally sampled by about 640 x 480 pixels in the case of the NTSC system, for example. Accordingly, it is a waste of the memory to prepare, for one kind of video picture, pixels of the number corresponding to that of the display screen of the display device. In the case of loading a scan converter function in the computer such as a PC or a WC, the style of an option board is taken most. Such an option board is required to be low in price, take small space for loading and consume low energy.

Fig. 3 schematically shows, in the structure of the video memory of the above-described literature, an operation from when video picture data is inputted in the graphics display device to when this video picture data is displayed on the display screen of the computer in the state a part of the video picture data is hidden by the other window.

In Fig. 3, 70 shows a display screen of the display device of a computer. In the display, a window 71 for displaying a video picture and a graphics display window 72 are partly superimposed with each other on the display screen 70. 20' shows a mask plane in which a mask pattern as shown has been written in advance by a processor (not shown) within the computer by referring to information relating to the layout of windows of the display screen.

In the mask plane 20', a hatched area 21 corresponds to a window 71 for displaying a video picture in the display screen 70, and mask information (1 bit, for example "0") at this portion shows a permit of writing of video picture data in the video VRAM plane. Mask information (1 bit, for example "1") in other area 22 shows a prohibition of writing of video picture data in the video VRAM plane.

The area 22 includes a cut portion 23 which corresponds to the portion of the window 71 hidden by the window 72 in the display screen 70.

10 schematically shows a memory capacity of the video picture data of 640 x 480 pixels. The inputted video picture data is sequentially written in the address corresponding to the window 71 on the display screen 70 of the video VRAM plane. In this case, writing of a part of the video picture data is prohibited by the mask information of the cut portion 23.

As described above, a video picture can also be cut in the structure of the video memory of the above-described literature. However, there is a problem in this structure that no consideration has been given to simultaneously displaying a plurality of kinds of video pictures on the display screen due to the fact that as a mask plane a masking memory of the capacity equivalent to that of the pixels of the display screen of the computer is necessary, that the masking memory and the video picture data are written within the same memory and that only one bit (1 plane) is provided as mask information of the mask plane.

Further, in the structure of the above-described literature, no consideration has been given to an expansion or a scaling down of a motion picture following an expansion or a scaling down of the window, and therefore, the size of the motion picture will not change even if the sizes of the window have been changed.

Considering the processing of the write control unit for controlling the writing of input video picture data into the video VRAM plane, the write control unit needs to generate a two-dimensional address, and a method of generating the address becomes complex when it is desired to carry out a scaling of an expansion or a scaling down of a video picture on the display screen or to carry out a reversed display, that is an inversion of up and down and right and left, of the video picture by applying a special effect. In the case of carrying out a scaling, the structure will become further complex when an occurrence of an alias (ruggedness in the display) is to be mitigated.

Further, when the user has changed the shape of the window on the display screen in the structure of the conventional video memory, it is necessary to update (rewrite) the mask pattern data of the mask plane in accordance with this change. However, if video picture data of the video VRAM plane has been rewritten in the middle of the updating of the mask pattern data, the video picture which is displayed becomes unnatural because considerable updating time is required. In general, during an updating of the mask pattern data, the stopping of the writing of the video picture data is considered. However, when the video picture is a motion picture, a stop motion results during the write stopping period.

Further, when the user has changed the shape of the window, the video picture data is written in a new window. In this case, if the video picture data so far been displayed in the window has not been deleted properly, the video picture data remains as a so-called "garbage data" in the display screen and the video VRAM plane, thus causing an inconvenient situation.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a video picture display device and a method for controlling the video picture display suitable for displaying a video picture in the computer system which employs a window environment.

It is another object of the present invention to provide a video picture display device and a method for controlling the video picture display which can perform a multiple picture processing in spite of a relatively simple structure.

In order to achieve the above-described objects, according to the preferred embodiments of the present invention, a masking memory is provided independent of a video VRAM in the video picture input unit and the mask data of the masking memory is corresponded to the number of pixels that structure the video picture.

Further, two mask memories may be provided in video picture input unit so that these mask memories are changed over at each end of video picture signal.

Further, the mask data of the masking memory may be divided into groups for each scanning line of relevant video picture input and information relating to position of the display screen and picture processing may be added to each group.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a configuration diagram of a first embodiment of the present invention.

Fig. 2 is an explanatory diagram for explaining the process up to the display according to the present invention.

Fig. 3 is a configuration diagram for explaining the display operation according to the prior art technique.

Fig. 4 is a configuration diagram of a second embodiment of the present invention.

Fig. 5 is a configuration diagram for showing one example of the masking memory structure.

Fig. 6 is a diagram for showing an example of the structure of the masking memory when the window in the display screen is further divided.

Fig. 7 is a configuration diagram for showing another example of the masking memory structure.

Fig. 8 is a configuration diagram of a third embodiment of the present invention.

Fig. 9 is a configuration diagram of a fourth embodiment of the present invention.

Fig. 10 is configuration diagram of a fifth embodiment of the present invention.

Fig. 11 is a memory configuration diagram for showing a sharing of the keying and mask data storing memories.

Fig. 12 is an explanatory diagram of the scaling system to which the straight line generation algorithm is applied.

Fig. 13 is an explanatory diagram for showing an example of the 1/2 scale down.

Fig. 14 is an explanatory diagram for showing an example of the 7/26 scale down.

Fig. 15 is a flow chart for showing one example of the straight line generation algorithm.

Fig. 16 is a flow chart for showing another example of the straight line generation algorithm.

Fig. 17 is a configuration diagram of a sixth embodiment of the present invention.

Fig. 18 is a configuration diagram of a seventh embodiment of the present invention.

Fig. 19 is a configuration diagram for showing an example of the pixel and line averaging unit.

Fig. 20 is a diagram for showing a detailed structure of pixel averaging in the embodiment shown in Fig. 19.

Fig. 21 is a diagram for showing an example of the weighting pattern for averaging which is used in the structure shown in Fig. 20.

Fig. 22 is a configuration diagram of an eighth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

At first, a first embodiment of the present invention will be explained with reference to Fig. 1 and Fig. 2.

Fig. 1 is a configuration diagram of the first embodiment of the present invention and Fig. 2 is an explanatory diagram for explaining the process until an input multi-media video picture is displayed. Referring to Fig. 1, 110 designates a video picture display device, 1 an input unit of multimedia video picture data such as a motion picture and a still picture, 3 a write control unit of a video VRAM 4, 2 a mask data storing memory, 5 a read control unit of the video VRAM 4, 8 a graphics display unit within a computer main body 100, the graphics display unit including a memory of a bit map corresponding to pixels that structure the display screen of the display device, 6 a change-over control unit for controlling pictures between the multi-media picture output of the video VRAM 4 and the graphics display output of the graphics

display unit 8, and 7 a display device within the computer main body 100. 101 designates a CPU within the computer main body 100. Fig. 2 is a diagram for explaining the data flow up to the stage where input data 10 of the picture data input unit 1 is displayed on a display screen 70 of the display device 7.

The mask data storing memory 2 in Fig. 1 has mask bits corresponding to the number of pixels of the video VRAM 4, and it is assumed that data as shown by mask data 20 in Fig. 2 has been written in advance in the mask data storing memory 2 by the CPU 101 within the main body. In Fig. 2, a hatched area 21 corresponds to a data display area (or a window) 71 of the multi-media video picture data in the display screen 70 of the display device 7, and this area is filled with information of mask disabling for writing the input video picture data 10 in the video VRAM 4. Other area 22 corresponds to a part of a graphics data display area 72 other than the multi-media data display area 71 in the display screen 70, and this area is filled with information of write mask for not writing the input data 10 in the video VRAM 4.

The write control unit 3 sequentially reads in advance the address of the mask data storing memory corresponding to the input video picture data 10. If the contents of the address is a mask disabling (area 21), the write control unit 3 operates so that the input data 10 is written in the video VRAM 4 and if the contents of the address is a write mask (area 22) the write control unit 3 operates so that the input video picture data 10 is not written in the video VRAM 4. In other words, the write control unit 3 for assigning the write position (address) to the video VRAM 4 reads the mask data of the masking memory 2 corresponding to the pixels of the video picture data and controls the writing by making decision whether the pixels are to be written in the VRAM 4 according to the contents of the read mask data. Based on this control, the input video picture data is clipped in the shape written in advance in the masking memory 2.

In the case of a television video signal, it is general that the television video signal is digitally sampled in about 640 x 480 pixel size in the case of the NTSC system, for example. Accordingly, if a write masking memory is available that has at most the capacity of the number of bits equal to that of the digital sample, it is possible to display the picture in a shape of a desired write area at a desired position even in the video VRAM that has a bit map (for example, 1280 x 1024) larger than the number of digital sample. In comparing the masking memory of this system with the above-described prior-art technique, the masking memory 2 shown in Fig. 1 requires a capacity of at most the number of the bits equal to that of the digital sample of the input video picture data, while the masking plane of the prior-art technique is integrated with the graphics VRAM and the masking plane requires the bit map of the size equal to that of the pixel structure of the display screen of the display device.

If a write masking memory 2 for allocating one bit to digital sample data of two pixels of an input video picture has been allocated, it is possible to further reduce the capacity of the write masking memory 2 to one half. To be more specific, it is more common that when a video picture input is to be digitalized in the display system of YUV (luminance, chrominance 1, chrominance 2) in stead of RGB (red, green, blue), for example, the chrominance component of the UV is sub-sampled. In this case, since one set of chrominance component UV becomes input data for two luminance component Y, it is more convenient to use two pixels as a unit for the write masking processing. In this case, it is possible to reduce the capacity of the write masking memory 2 to one half of the original capacity.

In general, when one bit of one-bit writing masking memory has been allocated to n-pixel digital sample data, the capacity of the write masking memory 2 can be reduced to one n-th of the digital sample number of the input data. More specifically, when the chrominance component has also been sampled in a vertical direction in the YUV display system as described above, or when one set of chrominance component UV becomes input data for the luminance component Y of total four pixels, including two pixels both vertically and laterally, it is more convenient to carry out the write masking processing based on four pixels as a unit. In this case, it is possible to reduce the capacity of the write masking memory 2 to one quarter of the original capacity. As described above, according to the present embodiment, the capacity of the write masking memory 2 can be minimized so that the cost relating to the memory can be reduced.

According to the prior-art technique, since the masking plane has been integrated with the video VRAM and the graphics VRAM shared memory, it has been necessary that the video VRAM 4 is read modified written when the write masking processing is performed. However, when the write masking memory 2 is separated from the video VRAM 4 as in the present embodiment, it is possible to carry out a pipe line processing by setting parallel the reading of the write masking memory 2 and the writing into the video VRAM 4, so that the bus band width of the video VRAM 4 can be improved to be about double in the case of writing other picture in the video VRAM 4. With this arrangement, there is an effect that a maximum number of

pictures that can be displayed simultaneously can be increased.

In many cases, a display of a plurality of motion picture windows is necessary in the video picture display device. The present invention can meet this requirement, and the present embodiment has a large effect of reducing the capacity of the write masking memory 2 which is necessary when a plurality of input units 1 are installed.

As descried above, it is general that a video signal such as a television signal is digitally sampled in the size of about 640 x 480 pixels in the case of the NTSC system, for example. Accordingly, if a write masking memory having the capacity of at most the number of bits equal to the number of digital samples is available, it is possible to display a video picture in the shape of a desired write area at a desired position even in the video VRAM having a bit map (for example, 1280 x 1024) which is larger than the number of the digital samples. In other words, a designation of a writing position id the video VRAM is carried out by a unit for assigning the write position of the picture, and the video picture is clipped in a shape written in advance in the write masking memory by a unit for reading the write masking memory according to the picture input and by a write control unit for controlling the writing by making a decision whether the picture input should be written in the VRAM or not according to the contents of the write masking memory.

A second embodiment of the present invention will be explained next with reference to Fig. 4, Fig. 5, Fig. 6 and Fig. 7. Fig. 4 is a configuration diagram of the second embodiment of the present invention in which a mask data storing unit 20 and a coordinate data storing unit 24 are provided in the masking memory 2. Referring to Fig. 4, 31 designates an address generating unit, 32 a unit for controlling the reading of coordinates / mask data, and 33 an address initialization control unit for the address generating unit 31. The address generating unit 31 is structured by an address resistor 34, a change-over unit 37, a ±1 arithmetic unit 36 and a ±1 arithmetic unit control resistor 35, as an example for generating a one dimensional writing address. Other units are the same as those provided with the same symbol marks in Fig. 1.

Fig. 5 shows one example of the configuration of the masking memory 2. The coordinate data storing unit 24 in Fig. 5 stores the coordinate data (address) of the video VRAM for writing picture data for each horizontal scanning of the input video picture data. In the coordinate data storing unit 24, the CPU 101 in the computer main body 100 stores in advance, as initial values, write starting coordinates (addresses) 240, 241, 242, 243, 244, 245, --- on the display screen 70 of the picture data of each horizontal line corresponding to each horizontal line of the video picture input. In the master data storing unit 20 which follows the coordinate data storing unit 24, the CPU also stores in advance write masking information 200, 201, 202, 203, 204, 205, --- for the video VRAM 4 that are determined according to the shapes of windows in the display screen 70.

Fig. 6 shows an example of other configuration of the masking memory 2. In Fig. 6, the CPU 101 within the computer main body 100 writes data in the masking memory 2 in the state that one window 71 on the display screen 70 is divided into four from the beginning. In other words, the mask data within the masking memory 2 is divided into four mask data groups of 20-1, 20-2, 20-3, and 20-4, and coordinate data on the video VRAM 4 is provided in each group for each horizontal scanning line of the video picture.

With this arrangement, when the video picture input is a result of a combination of a plurality of video pictures, the divided window portions can be freely moved within the range of the data write range of each video VRAM 4 when the coordinate data of each mask data is rewritten from the video picture display device side.

If the window 71 is to be used as the original one window, the coordinate data added to each group is determined so that the end of the left side mask data group is connected to the starting of the right side mask data group for each horizontal line of the input video picture. It is needless to mention that although Fig. 6 shows an example of one window divided into four, the window can be divided into any desired number.

Fig. 7 shows another example of the configuration of the masking memory 2. In the coordinate data storing unit 24 of Fig. 7, an address scanning direction of the horizontal line on the video VRAM 4 that is generated by the address generator 31, that is, direction flags 250, 251, 252, 253, 254, 255, --- for assigning + (a scan in the right direction) or - (a scan in the left direction) are stored in advance, in addition to the write starting coordinates (addresses) 240, 241, 242, 243, 244, 245, --- on the video VRAM 4 of the picture data of each horizontal line corresponding to each horizontal line of the picture input. The contents of the mask data storing unit 20 that follow the coordinate data storing unit 24 are the same as those explained with reference to Fig. 5.

The operation will be explained next with reference to Fig. 4 and Fig. 7. The control unit 32 for controlling the reading of coordinates / mask data sequentially reads one line data of the coordinates memory storing unit 24 of the masking memory 2, that is, the direction control flag 250 and the write starting coordinates 24. The read data are inputted

to the address initialization control unit 33. The address initialization control unit 33 sets the contents of the direction control flag 250 in the ±1 arithmetic unit control register 35 and then sets the address based on the contents of the write starting coordinates 240 in the address register 34 based on the change-over unit 37.

Then, the control unit 32 for controlling the reading of coordinates / mask data controls the writing by determining whether the data from the picture input unit 1 is to be written in the video VRAM 4 or not by reading the mask data 200. In synchronization with this, the address generating unit 31 generates a write address to the video VRAM by adding one to or subtracting one from the contents of the address register 34 according to the contents of the direction control flag 250, with the address based on the contents of the write starting coordinates 240 set as an initial value. Thereafter, each time when the processing for one line has been completed, the coordinate / mask data read controlling unit 32 proceeds the processing by reading a direction control flag 251, a write starting coordinates 241, --- corresponding to the next line.

As described above, according to the present embodiment, it is possible to develop inputted picture data in a desired direction from a desired position in a line unit by storing in advance, in the coordinate data storing unit 24, the write starting coordinates to the video VRAM 4 and the writing direction. In other words, when the coordinate data has been set so as to write sequentially from the top downwards in the coordinate data storing unit 24 as explained above, the coordinate data are exploded from top to down. If the coordinate data has been set so as to perform writing in the opposite direction, the coordinate data are exploded from bottom upwards. Therefore, an up and down inverse display of the picture data can be performed easily. Further, when the direction flags 250, 251, 252, 253, 254, 255, --- to be stored in the arithmetic unit control register 35 are rewritten, the picture data are exploded from the right to the left by generating the addresses from the right to the left by the address generator 31. When the addresses are generated from the left to the right, the picture data are also exploded from the left to the right. Therefore, the left and right inversion display can be performed with ease. It is, of course, possible to control these for each line so that these can also be applied to obtain a special effect. Further, since it is sufficient that the address generator 31 generates only addresses for one line, it is not only possible to reduce the scale of the logical circuit that structures the address generator but also there is an effect that a more complex address can be generated.

The system for executing the control data by reading them in a line unit as described in the present embodiment can also be expanded as shown in Fig. 6. In other words, by equally dividing one line into m, a coordinate data storing unit 24 and a mask data storing unit 20 shown in Fig. 5 and Fig. 7 are provided corresponding to each line of the l/m length. To be more specific, the masking memory 2 shown in Fig. 5 and Fig. 7 is arranged by m number in the horizontal direction so that the coordinate / mask data read control unit 32 reads the coordinate storing unit 24 and the mask data storing unit 20 in the unit of l/m of one line to perform the processing. With the above-described arrangement, it is possible to display an input dynamic data of one screen by dividing the data into m parts in the horizontal direction.

In the case of a division of data into a vertical direction, the data can be divided in one line unit by merely changing the coordinate data stored in the coordinate data storing unit as described above. For example, when the vertical direction has been divided into p, an input one screen of dynamic data is divided into small screens of p x m pieces and the data stored in the mask data storing unit 20 is changed to make it possible to make a superimposed display of motion pictures on the respective small screens. In this case, the coordinate / mask data read control unit 32, the address initialization control unit 33 and the address generator 31 can share the processing of m times for all the processing so that the display of a screen data divided into p x m small screens is made possible without an increase in the number of the control circuit. If p x m small screens have been combined before the dynamic data is inputted, it is possible to provide, by using this function, a device in a single input picture display device which is equivalent to the multi-input picture display device. This multiple function is a large effect that can be obtained by the present embodiment.

A third embodiment of the present invention will be explained next. Fig. 8 is a configuration diagram for showing the third embodiment of the present invention that has two write mask data storing units. In Fig. 8, 25 designates a mask A, 26 a mask B, and each mask may be added with a coordinate data storing unit shown in Fig. 5 and Fig. 7. 41 designates a mask change-over instruction register, 42 a vertical timing generator, 43 a D flip-flop, 44 a pointer A for generating a reading address for the mask A 25, 45 a pointer B for generating a reading address for the mask B 26, and 46 a selector for changing over between the pointer A 44 and the pointer B 45. The other units are the same as those having the same symbol marks in Fig. 1 to Fig. 7.

It is necessary to have at least two write mask data memories. By referring to a state display flag that shows a state of the selector 46 which is the change-over control unit for the mask A 25 and the mask B 26 that are the write mask data storing units, if the input video picture is being displayed by using the mask A 25 which is the first write mask data storing unit, it is possible to write new write mask data in the mask B 26 which is another write mask data storing unit.

When the writing of the mask data has been finished, the change-over instruction register 41 which is a change-over instruction unit of the mask data storing unit instructs a change-over from the mask A 25 to the mask B 26. Upon knowing the instruction of the change-over given by the change-over instruction register 41, the selector 46 changes over between the mask A 25 and the mask B 26 based on a synchronization timing signal sent from the vertical synchronization timing generator 42 that generates a timing which is synchronous with the vertical synchronization signal of the input motion picture, and then changes the state of the flag. The change-over of the mask data storing units is carried out immediately in the timing synchro nous with the vertical synchronization signal of the input motion picture, as described above.

The detailed operation will be explained next. To simplify the explanation, it is assumed that write mask information corresponding to the picture input currently being displayed is being set to the mask A 25 as an initial state and that the pointer A 44 has been selected by the change-over instruction register 41 and the selector 46. It is also assumed that the state in this case is being reflected in the state display flag which is an output of the D flip-flop 43. When it has become necessary to change the shape of the mask based on the operation of the user, a control unit such as a processor (not shown, and hereinafter to be simply referred to as a "processor") checks the state display flag of the output of the D flip-flop 43 and it is recognized that the current mask A 25 is currently in the active state. The processor writes new mask information in the mask B 26 and, when this has been finished, rewrites the contents of the change-over instruction register 41 so that the mask B 26 is selected. The contents of the change-over instruction register 41 are held until when the vertical synchroniza tion timing generator 42 generates a timing signal synchronous with the vertical synchronization signal from the picture data input unit 1. The generation of the timing signal synchronous with the vertical synchronization signal is awaited in this case in order to wait for a completion of the explosion of one-frame or one-field picture data in the video VRAM 4. When a timing signal synchronous with the vertical synchroniza tion signal has been generated, the contents of the change-over instruction register 41 are reflected in the output of the D flip-flop 43, the pointer B 45 is selected by the selector 46 and the change-over to the mask B 26 has been completed. A change-over from the mask B 26 to the mask A 25 can also be achieved in the similar procedure.

As described above, according to the present embodiment, a change-over between the mask A 25 and mask B 26 can be effected immediately in the timing synchronous with the vertical synchronization signal of the input motion picture. Therefore, the contents of the video VRAM can not be rewritten carelessly by incomplete mask data or the motion picture currently being displayed can not be placed in a stopped motion.

Because of the above-described characteristics, there is an effect that whole picture data can be obtained without a loss unlike a loss of dynamic data during a stopped motion experienced in the past. This effect is very important, particularly in the case of picture data obtained from a broadcasting program, because most of such picture data can not be retransmitted.

A fourth embodiment of the present invention will be explained next. Fig. 9 shows a configuration diagram for showing the fourth embodiment of the present invention according to which picture data already written in the window by an old mask of the video VRAM 4 can be deleted automatically when the write mask data has been changed over. In Fig. 9, 47 designates a shift register and 48 designates a color data change-over unit for changing over between the picture data from the picture data input unit 1 and specific color data. Other units are the same as those with the same symbol marks shown in Fig. 8.

At least two mask data storing units are provided. Accordingly, by referring to the state display flag for showing the state of the selector 46, if the mask A 25 is being used to carry out a display of a picture, new mask data is to be written in the mask B 26 which is another write mask data storing unit. When the writing of the mask data has been finished, the change-over instruction register 41 instructs a change-over from the mask A 25 to the mask B 26. The operation up to this stage is the same as that of Fig. 8.

Upon knowing the instruction of change-over given by the change-over instruction register 41, the selector 46 forcibly changes over the input dynamic data to data of a specific color after waiting for a synchronization timing signal from the vertical synchronization timing generator 42 which generates a timing synchronous with the vertical synchronization signal of the input motion picture. The data of the specific color is the data of a color

which is used to delete a picture such as a black color, for example. The selector 46 further waits for a synchronization timing signal from the vertical synchronization timing generator 42 to change over between the mask A 25 and the mask 26 to change the state of the state display flag. During this period, the deletion of the picture data in the area in which the dynamic data has been written is completed and therefore, the "garbage data" can be securely deleted at the moment when the write area of the motion picture changes.

A detailed operation will be explained next. To simplify the explanation, as in the case of the preceding embodiment, it is assumed that write masking information corresponding to the picture input currently being displayed has been set in the mask A 25 and that the pointer A 44 has been selected by the change-over instructing register 41 and the selector 46. It is also assumed that the status in this case has been reflected in the status display flag which is the output of the D flip-flop 43. When it becomes necessary to change the shape of the mask by the operation of the user, the processor checks the status display flag of the output of the D flip-flop 43 to recognize that the mask A 25 is currently in the active state. The processor writes new mask information to the mask B 26, and after finishing the writing, rewrites the contents of the change-over instruction register 41 so that the mask B 26 is to be selected. The contents of the change-over instruction register 41 are held until the timing signal synchronous with the vertical synchronization signal from the picture data input unit 1 has been generated three times from the vertical synchronization timing generator 42. The generation of the timing signal synchronous with a first vertical synchronization signal is awaited in order to wait for the completion of the explosion of the picture data of the first field in the video VRAM 4.

A signal of the intermediate tap of the shift register 47 that has been changed as a result is inputted to the color data change-over unit 48. After a timing signal which is synchronous with the vertical synchronization signal has been generated by further two times, that is, after one-frame time has elapsed, the contents of the change-over instruction register 41 are reflected in the output of the D flip-flop 43 and the pointer B 45 is selected by the selector 46, thus completing the change-over to the mask B 26.

As is clear from the above explanation, during the period from when the signal of the intermediate tap of the shift register 47 changed to when the signal of the status display flag which is the output of the D flip-flop 43 has changed, both signals which are supplied to the color data change-over unit 48 take different values. The fact that both signals take different values can be detected by an exclusive logical sum or other unit. Therefore, based on the result of this detection, the color data change-over unit 48 takes the data of the picture input unit 1 if the values of both signals are the same, and operates to output specific color data in stead of the data of the picture input unit 1 if the values of both signals are different. The specific color refers to the color to be used at the time of deleting the picture, like a black color, as described before. Since the input of the specific color continues during the period of the input of the picture of one frame, the area of the mask A 25 which has been used so far is completely refilled with the specific color, thus completing the deletion. A change-over from the mask B 26 to the mask A 25 can also be achieved in a similar manner.

As described above, according to the present embodiment, the picture data in the mask area which has so far been used until the change-over between the mask A 25 and the mask B 26 can be deleted automatically. Accordingly, the load of the software can be reduced and the deletion can be made at the timing synchronous with the input of the picture. Therefore, there is an effect that no unnecessary flickering occurs and that an automatic deletion function can be added with an extremely small number of circuits.

Next, a fifth embodiment of the present invention will be explained with reference to Fig. 10 and Fig. 11. Fig. 10 is a block configuration diagram of the fifth embodiment of the present invention. In Fig. 10, 2 designates a mask data storing memory, 9 a keying data storing memory, and 11 a keying and mask data storing memory. Other units are the same as those having the same symbol marks in Fig. 1.

The keying data will be explained first. The picture change-over control unit 6 changes over between the picture data from the video VRAM 4 and the graphics display data from the graphics display unit 8. In this case, information for showing which data should be selected at this change-over stage is the keying data. The keying data is stored in the keying data storing memory 9. The read control unit 5 of the video VRAM reads the keying data storing memory 9 in synchronization with the reading of the video VRAM 4. In the present embodiment, the keying data storing memory 9 and the mask data storing memory 2 are being shared by the keying and masking data storing memory 11.

Normally, the video VRAM 4 and the keying and masking data storing memory 11 are structured by using a multi-port memory having at least the random access memory (RAM) and the serial access memory (SAM). What is important in this case is that the keying data from the keying data

storing memory 9 to the picture change-over unit 6 is transmitted through the SAM unit of the keying and masking data storing memory 11 and the masking data from the masking data storing memory 2 to the write control unit 3 of the video VRAM is trans mitted through the RAM unit of the keying and mask data storing memory 11, in order to transmit the picture data from the video VRAM 4 to the picture change-over control unit 6 through the SAM unit of the video VRAM 4. With the above arrangement, the mask data storing memory 2 and the keying data storing memory 9 can be shared to form the keying and masking data storing memory 11.

An example of the bit map of the keying and masking data storing memory 11 is shown in Fig. 11. The keying and masking data storing memory 11 has a bit map of 2048 x 1024, of which 1280 x 1024 bits are used for the keying data storing memory 9 with the rest for the mask data storing memory 2. A half of the mask data storing memory 2 is used for the mask A 25 and the remaining half for the mask B 26. Normally, the memory is loaded in a value of a power of 2 such as 2048 x 1024. As is clear from Fig. 11, a spare area of the keying data storing memory 9 can not only be efficiently used for the masking data storing memory 2 but also be shared to reduce the size of the memory elements. Therefore, there is an effect that the device can be provided at low price and power consumption for the device can be reduced.

According to the present invention, a video picture displayed on the window of the display screen can be scaled to be expanded and compressed within the window. Particularly in the present invention, an evident effect can be obtained for the scaling down.

A scaling down scaling can be achieved by a thinning of pixels in the horizontal direction and by a thinning of horizontal lines in the vertical direction.

A sixth embodiment of the present invention will be explained next. In the present embodiment, the input video picture is scaled by using a line generator. The line generator of the present embodiment is characterized in that the pixels or horizontal line to be thinned is determined by using a known oblique line generation algorithm. Fig. 15 shows one example of the oblique line generation algorithm of the line generator and Fig. 16 shows another example of the oblique line generation algorithm. In Fig. 15, A designates an error accumulator, n a quotient obtained by dividing a number x of the input picture data by a number y of output data after a scale down, and r a remainder in this case. Fig. 15 shows a processing for drawing a horizontal line component which is structured by (n + 1) dots when a value of an accumulated error has exceeded 1 after an error less than one dot has been accumulated by r each time when a horizontal line component structured by n dots is drawn. At an initialization processing step 100, the value of the error accumulator A is set to 0. At an error accumulation processing step 101, the value r for showing an error of less than one dot per one time is added to the error accumulator A. At a condition decision processing step 102, a decision is made whether a resultant accumulated error has exceeded 1 or not. If the accumulated error has exceeded 1, the exceeded 1 is subtracted at an accumulated value correction processing step 103, and an output processing of (n +1) is executed at a step 104. If the accumulated error has not exceeded 1, an (n) output processing is executed at step 105.

Depending on the values of x and y, the above r may become a recurring decimal and there may occur an error at the time of an accumulation. An example of Fig. 16 takes this case into account and facilitates to solve this problem in the hardware. In Fig. 16, R is a result of a rationalization by multiplying r by y. By carrying out this processing, the processing for drawing a horizontal line component structured by (n + 1) dots when the value of the accumulated errors in the error accumulator A has exceeded y, that is, an (n + 1) output processing, is carried out at step 114. Further, in order to simplify the condition decision processing step 112, y is subtracted in advance at the initialization processing step 110. With this arrangement, at the condition decision processing step 112, A is not compared with y but A is compared with O.

In summary, at the initialization processing step 110, the value of the error accumulator A is set to -y. At the error accumulation processing step 111, the value R for showing the error less than y (1 dot) at one time is added to the error accumulator A. At the condition decision processing step 112, a decision is made whether the resultant accumulated error has exceeded 0 or not. If the accumulated error has exceeded 0, the exceeded y is subtracted at the accumulated value correction processing step 113, and the (n + 1) output processing is carried out at the step 114. If the accumulated error has not exceeded 0, the (n) output processing is carried out at the step 115.

Fig. 17 is a block configuration diagram of the sixth embodiment of the present invention. In Fig. 17, 51 designates a horizontal line generator, 52 a pixel selector, 53 a vertical line generator, and 54 a line selector. Other units are the same as the units having the same symbol marks in Fig. 5. As described above, the scaling down scaling can be achieved by thinning the pixels in the horizontal direction and by thinning the horizontal lines in the vertical direction.

(1) thinning of pixels in the horizontal direction

Referring to Fig. 12, consider the case that a straight line is to be drawn from an origin (0, 0) to a point (x - 1, y - l) in the first quadrant of an xy orthogonal coordinates system, where x and y are integers respectively and x corresponds to the number of picture data of picture input and y corresponds to the number of pixel data after scaling down scaling for writing into the video VRAM. It is assumed that each dot for structuring a straight line can be drawn only at a position of an integer value of a coordinate axis. Now, since a scaling down scaling is being considered, there is a relationship of $x \geqq y$ and an angle θ to be formed by the straight line and the x axis is $0 \geqq \theta \geq 45°$,

If the straight line is drawn by using a known oblique line drawing algorithm, the straight line can be expressed as a set of y horizontal line components of at least one dot. In this case, the length of each horizontal line component can be considered to represent the number of pixel data of a picture input corresponding to one pixel data after the scaling down scaling for writing into the video VRAM. The length of individual horizontal line component may be different, when a window has a cut-out portion, for example, or all the horizontal line components may have the same length. In general, if the length of each horizontal line is expressed as n, the scaling down scaling in the horizontal direction can be achieved when one pixel data is selected from the picture data of n picture inputs by using the pixel selector 52 and the selected pixel data is written in the video VRAM 4.

Fig. 13 shows an example of a half scale down, where it is assumed that 26 input data is compressed to a half, that is, 13 input data, for example. The length n of the 13 horizontal line components for structuring the straight line becomes 2, which shows that one output may be selected for two input pixel data. Fig. 14 shows an example of a 7/26 scale down, which assumes that 26 input data are to be compressed to 7 input data. The length n of the 7 horizontal line components for structuring the straight line, that is, the number of pixels, becomes 3 or 4, which shows that one output may be selected for three or four input pixel data. Thus, the horizontal line generator 51 generates the length n of the y horizontal line components per one line and gives this number n to the pixel selector 52 and also gives address update information of the y times to the address generator 31. The pixel selector 52 selects one pixel data from the n pixel data from the input unit 1 based on the given number n, and gives the selected data to the next line selector 54. In selecting data, either the first data or the last data may be selected, or the intermediate data may be selected.

(2) thinning of horizontal lines in the vertical direction

When the scanning system is the one for sequentially scanning the picture input in the order from the top downwards as in the case of the non-interlace system, the processing similar to the one described above is also carried out in the vertical direction. When the scanning system is the interlace system, that is the skip scanning system, lines to be thinned are determined in advance by using the vertical line generator 53 and picture data to be inputted in the horizontal unit is controlled by determining whether the picture data is to be written in the VRAM 4 for each horizontal line or not, and writing of the lines to be thinned in the video VRAM is prohibited. The vertical line generator 53 generates a length n' of y' horizontal line components per one field as described above and gives the length n' to the line selector 54. The line selector 54 selects pixel data of one line from the pixel data of n' lines from the pixel selector 52 based on the given n', and gives the selected data to the video VRAM 4. In selecting lines, either the first lines or the last lines may be selected, or the intermediate lines may be selected. For the selected lines to be written in the video VRAM 4, the scaling down scaling in the vertical direction can be achieved by setting write starting coordinates so that only the selected lines can continue in the vertical direction in the coordinates data storing unit 24 described in the second embodiment of the present invention.

As described above, according to the present embodiment, motion picture data can be scaled into a desired size so that there is an effect that multi-media data can be freely displayed in the window environment.

It is also good, as described in the second embodiment of the present invention, to store in advance initial values necessary for the horizontal line generator 51, the vertical line generator 53 or the pixel selector 52, in the coordinates data storing unit 24 for the mask data storing memory 2, and to initialize at the beginning of each line by the coordinates / master data read controlling unit 32. Particularly, the line selector 54 needs only information on whether the current lines are necessary or not and, therefore, there is an effect that the vertical line generator 53 can be omitted. Further, since the initial value of scaling can be changed in line unit, it becomes possible to have a more complex special effect, such as a trapezoidal display of a dynamic window or a mapping in an area covered by a curve. Similarly, by combining the effect of the present embodiment with the split control function of small screens of p x m described in the second embodiment, it is possible to

have an independent scaling in the respective small screens. In this case, it is also possible to have a multi-function without a substantial alteration to the control circuit.

Next, a seventh embodiment of the present invention will be explained with reference to Figs. 18 to 21. While in the sixth embodiment of the present invention, one pixel data has been selected from the pixel data of n picture input data by using the pixel selector 52 or the line selector 54 and the remaining pixel data has been abandoned, a picture filtering processing will be carried out to mitigate the occurrence of an alias (a ruggedness in the display) in the seventh embodiment of the present invention. In Fig. 18, 55 designates a pixel averaging unit in place of the pixel selector used in Fig. 7 and 56 designates a line averaging unit in place of the line selector 54 used in Fig. 17. Other units are the same as those having the same symbol marks in Fig. 17. Fig. 19 is a block configuration diagram for showing an example of the pixel averaging unit 55 and the line averaging unit 56. In Fig. 19, 551 designates a pixel input weighting unit, 552 a pixel adder, 553 a register for the accumulator, 554 a pixel gate, 555 a pixel output shifter, 556 a pixel average control unit, 561 a line input weighting unit, 562 a line adder, 563 a line buffer, 564 a line gate, 565 a line output shifter, and 566 line average control unit.

(1) picture filtering processing in the horizontal direction

For the value n outputted by the horizontal line generator 51 in place of the pixel selector 52, the pixel averaging unit 55 arranges the pixel data of n dots of the picture input to average the n-dot pixel data of the picture input, thus performing the picture filtering processing in the horizontal direction. The horizontal line generator 51 generates the length n of y horizontal line components per one line as described above and gives the length n to the pixel average control unit 556 of the pixel selector 52 and, at the same time, gives address updating information of y times to the address generator 31. Inside the pixel averaging unit 55, the pixel average control unit 556 averages the n pixel data from the input unit 1 based on the given value n, and controls to give the averaged result to the next line averaging unit 56. In other words, the pixel input weighting unit 551 sets the input data to be multiplied by one or two by the shifter, and the adder 552 adds the result to the contents of the accumulator 553, thus accumulating the values in the accumulator 553. The pixel gate 554 is for giving the initial value of the accumulator 553 and is controlled by the pixel average control unit 556 to output data of 0 for the first pixel of the given n. The pixel average control unit 556 controls the pixel input weighting unit 551 so that the sum of the weight of the accumulated values becomes a power of 2 when the accumulation of the n pixels has been finished. The pixel output shifter 555 is controlled by the pixel average control unit 556 to carry out a right shifting so that the weight is returned to 1 when the accumulation of the n pixels has been completed. With the above arrangement, the n dot pixel data of the picture input are averaged to achieve the picture filtering in the horizontal direction.

A further detailed configuration example of the pixel average control unit 556 and one example of the control method therefor will be explained with reference to Fig. 20 and Fig. 21. Fig. 20 shows an example of the configuration of the pixel average control unit and Fig. 21 shows an example of the pixel average control method using this pixel average control unit. How the pixel average control unit 556 controls to set the weight of the accumulated value of n input pixels to a power of 2 and how the pixel output shifter 555 returns the weight to 1 will be explained below based on the cases of the input pixel n = 6 and n = 13 respectively.

606 schematically shows how six input pixels are weighted when n = 6. Six rectangles correspond to six input pixels and height of each rectangle shows a weighting. Assume that the rectangles of a smaller height shows the weight of 1 and the rectangles of a larger height shows the weight of 2. Assume that the rectangle at the right end shows the first input pixel and then the second, third, ---, and sixth pixels from the right to the left are to be inputted in this order. This shows that when n = 6, or when the six input pixels are averaged, the weights of the input pixels are 1, 1, 2, 2, 1, 1 respectively so that the sum of the weights is 8 which is 2 to the third power, that is, 2^3.

When n = 13, or when 13 input pixels are averaged, the weighting of the respective input pixels is made to be such that the weight of 1 is repeated five times, 2 is repeated three times and 1 is repeated five times in this order so that the sum of the weights is 16 which is 2 to the fourth power.

As described above, it is possible to put a plurality of input pixels into one set by accumulating the inputs by multiplying the inputs by one or two and then by multiplying the sum by a minus power of 2. With this arrangement, it is possible to set the hardware structure for averaging in a very simple structure. It is assumed here that the operation of putting a plurality of input pixels into one set is expressed as averaging.

Fig. 21 shows a case the n is other number. Fig. 21 shows an example of the method for weigh-

ting when n is 1 (601) to n is 31 (631), and it can be easily confirmed that by implementing the weighting as shown in Fig. 21, all the sums become 2 to the power of some number.

The structure shown in Fig. 20 is the structure for performing the averaging control by weighting based on the method as shown in Fig. 21. In Fig. 20, those units having the same symbol marks as those in Fig. 19 are the same units. In other words, 551 designates the pixel input weighting unit, 552 the adder, 553 the accumulator, 554 the pixel gate, 555 the pixel output shifter, and 556 the pixel average control unit. 570 designate a control signal generator, 571 a change-over unit, 572 a decrementer, 573 a register, 574 a zero detector, 575 and 576 comparators and 577 an OR gate.

The change-over unit 571, the decrementer 572, the register 573 and the zero detector 574 constitute a down-counter, and the comparators 575 and 576 and the OR gate 577 constitute a window comparator. By loading the given value of n and down counting for each input of the pixels, the down-counter generates n outputs from (n -1) to 0 as described later and specifies the order of the current input pixel among the total input pixels so far. The window comparator generates a weight control signal 585 for controlling to determine the weight of 1 or 2 to each pixel. The control signal generator 570 outputs an upper limit value signal line 583 to be given to the comparator 575 for comparing the upper value at the window comparator, a lower limit value signal line 582 to be given to the comparator 576 for comparing the lower limit value, and a shift value control line 586 of the pixel output shifter 555, based on the data value of n inputted from a signal line 580, respectively.

A table inside the block of the control signal generator 570 shows an outline of how and what signal the control signal generator 570 generates each time based on the value of the data n inputted from the signal line 580. For the sake of simplicity, it is assumed that the value of n ranges from 1 to 31 and the tables shows which value each signal line takes within each range of data value n of 1, 2 to 3, 4 to 7, 8 to 15, and 16 to 31. Figures shown in the column of the shifter show fractions into which each value accumulated in the accumulator 553 within each range of the value of n shown on the left side is to be finally shifted by the picture output shifter 555 (reference Fig. 21). D4 to D0 show the n values expressed in binary numbers and x shows a portion which changes into 0 or 1 based on the value of n shown on the left end. S4 to S0 which are the upper value signal lines 583 are the values of only the highest order 1 being taken out from the D4 to D0 which are the signal lines 580, and a person engaged in this business can easily produce these values from the D4 to D0 by using a known technique known as a priority encoder. L4 to L0 which are the lower limit value signal lines 582 are the highest order 1 of the D4 to D0 changed to 0, and these values can be generated by carrying out an exclusive logical sum of the D4 to D0 and the S4 to S0. By comparing the necessary shift values shown in the column of the shifter with the values generated by the S4 to S0, it can be known that these values correspond to each other at 1 to 1. Therefore, a person engaged in this business can easily understand that the S4 to S0 can be used as they are or the shift value control lines 586 can be generated with some conversion.

The operation when n is 6 will be explained in order. When n is 6, the D4 to D0 become "00110" and the S4 to S0 of the upper limit value signal lines 583 become "00100" because only the highest order 1 of the D4 to D0 is taken out. The L4 to L0 of the lowest limit value signal lines 582 become "00010" because the highest order 1 of the D4 to D0 is changed to 0. Further, based on the values of the S4 to S0, the shift value control lines 586 output the values which make the pixel output shifter 555 to carry out the shifting of 1/8. When the initial value of the register 573 at the down-counter is 0, the zero detector 574 detects 0 and controls the change-over unit 571 to input the value of n "00110" to the decrementer 572. The decrementer 572 outputs to the register 573 the value "00101" which is the result of the input subtracted by 1. After this value has been loaded to the register 573 and the output values of the C4 to C0 of the register 573 have become "00101", the zero detector 574 controls the change-over unit 571 to input the output values of the register 573 to the decrementer 572. Thereafter, down counting is continued until the output values of the C4 to C0 of the register 573 have become 0. This state is shown in C4 to C0. Next, the comparator 575 for structuring the window comparator always compares the S4 to S0 of the upper limit signal lines 583 (the value in this case is "00100") with the outputs C4 to C0 of the register 573 and outputs H during the first two pixels period. Further, the comparator 576 always compares the L4 to L0 of the lower limit signal lines 582 (the value in this case is "00010") with the outputs C4 to C0 of the register 573 and outputs H during the last two pixels period. The results of these are logically summed by the OR gate 577, and L is outputted during the intermediate two pixels components period during which the H is not being outputted by the comparators 575 and 576. With the above arrangement, it is possible to generate the desired weight control signal 585 when n is 6.

The operation when n is 13 will be explained below. When n is 13, the D4 to D0 become

"01101" and the S4 to S0 of the upper limit value signal lines 583 become "01000". The L4 to L0 of the lowest limit value signal lines 582 become "00101". Further, based on the values of the S4 to S0, the shift value control lines 586 output the values which make the pixel output shifter 555 to carry out the shifting of 1/16. When the initial value of the register 573 at the down-counter is 0, the decrementer 572 outputs the value "01100" which is the result of the input value n subtracted by 1. After this value has been loaded to the register 573, down counting is continued until the output values of the C4 to C0 of the register 573 have become 0. This state is shown in C4 to C0. Next, the comparator 575 always compares the S4 to S0 of the upper limit value signal lines 583 (the value in this case is "01000") with the outputs C4 to C0 of the register 573 and outputs H during the first five pixels period. Further, the comparator 576 always compares the L4 to L0 of the lower limit value signal lines 582 (the value in this case is "00101") with the outputs C4 to C0 of the register 573 and outputs H during the last five pixels period. The results of these are logically summed by the OR gate 577, and L is outputted during the intermediate three pixels components period during which the H is not being outputted by the comparators 575 and 576. With the above arrangement, it is possible to generate the desired weight control signal 585 when n is 13.

Based on the above-described procedures, it will be easily understood that the pixel average control unit 556 can generate desired control signal groups when n is other than 6 or 13.

(2) picture filtering processing in the vertical direction

The line averaging unit 56 averages the pixel data included in a plurality of lines in the vertical direction and achieves the picture filtering processing in the vertical direction. The operation is the same as the above-described processing in the horizontal direction except that the processing is in line unit. In averaging the pixel data, based on the n' from the vertical line generator 53, the line input weighting unit 561 weights each line for each data of the n' lines for which the above-described picture filtering processing in the horizontal direction has been carried out. The line adder 562 stores the accumulation result in the line buffer 563. The line gate 564 is used to prevent the data from the line buffer 563 from being inputted to the line adder 562 for the first line of the n' lines which are to be compressed. In accumulating the n'-th line to be compressed, the accumulation is carried out so that the sum of the weighting becomes 2 to the power of some number, and the accumulation is controlled by the line output shifter 565 so that the weight becomes 1. The result of the control is written in the video VRAM 4 by using the horizontal unit write control unit, thus achieving the pixel data averaging both in the horizontal direction and the vertical direction.

As described above, according to the present embodiment, it is possible to carry out scaling while carrying out the picture filtering processing of the input dynamic data in desired sizes, so that there is an effect that the multi-media data can be displayed in high quality in the window environment.

Further, as described in the sixth embodiment of the present invention, it is also good to initialize each line by the coordinates / mask data read control unit 32 by storing in advance the initial values which are necessary for the horizontal line generator 51, the vertical line generator 53 or the line averaging unit 56 in the coordinates data storing unit 24 of the mask data storing memory 2. Particularly, the line averaging unit 56 requires only the information of whether the current lines are necessary and information of input weighting coefficient and line buffer output coefficient, so that there is an effect that the vertical line generator 53 can be omitted and the line average control unit 566 can be replaced by a simple register. Further, since the initial value of the scaling can be changed in line unit, a more complex special effect can be obtained such as, for example, a trapezoidal display of the dynamic window or a mapping in the area encircled by a curve is made possible. Similarly, in combination with the p x m small screen split control function as descried in the second embodiment, it is needless to mention that the scaling can be carried out independently while performing the picture filtering in the small screen unit. A multi-function can also be obtained in this case without a substantial change in the control circuit.

An eighth embodiment of the present invention will be explained with reference to Fig. 22. Fig. 22 is a block configuration diagram of the eighth embodiment of the present invention. Referring to Fig. 22, three video pictures of a picture data input unit A 12, a picture data input unit B 13 and a picture data input unit C 14 are inputted. Although the number of the input video pictures is assumed to be three in the present embodiment, it is needless to mention that the present invention can be applied to any desired number of at least two input video pictures. 2' designates a mask data storing memory having a 2-bit depth, and this mask data storing memory has a mask plane 2-1 for storing mask data of a first bit position and a mask plane 2-2 for storing mask data of a second bit position. Other units are the same as those units having the

same symbol marks shown in Fig. 1. Each of a video VRAM 4', the mask planes 2-1 and 2-2 has bit a number corresponding to the number of pixels of the display screen 70 of the display device 7.

In the mask data storing memory 2' having the same bit map as that of the graphics VRAM 4' and having a depth of a plurality bits, one of the plurality of picture input numbers can be written, as in the case of the color display in the conventional graphics VRAM. For example, it is possible to express four ways in the masking memory having a 2-bit depth and 256 ways in the masking memory having an 8-bit depth. Normally, one way is allocated to the graphics display and no allocation is made to correspond to any picture data input for the video VRAM. Accordingly, the maximum number of picture data input units that can be handled in the mask data storing memory 2 having the n-bit depth becomes 2 to the power of n - 1. In the plurality of picture data input unit, picture input numbers are defined exclusively in the respective picture data inputs corresponding to each picture data input unit. For example, the input unit A 12 has "01", the input unit B 13 has "10" and the input unit C 14 has "11", in the binary unit respectively. "00" has been allocated to the graphics VRA within the graphics display unit 8. Which input picture is to be displayed at what position on the display screen within the computer main body is determined by assigning the picture input number in 2 bits using two mask planes for each pixel on the display screen. The CPU within the computer main body writes in advance the mask data in the two mask planes 2-1 and 2-2 as in the case of the preceding embodiments.

The video VRAM write control unit 3 reads the mask data storing memory 1' corresponding to the coordinates of the video VRAM 4' into which the inputted pixel data is to be written. In this case, a detection of coincidence between the picture input number defined in the picture data input unit and the contents of the write mask data storing memory 2' is carried out. If the defined picture input number coincides with the contents of the write mask data storing memory 2', the video VRAM write control unit 3 writes the picture data in the video VRAM 4. It is only sufficient to fill in the window square area with the data of the picture input number in the write mask data storing memory 2 just like drawing a window in the conventional graphics VRAM. At most one number can be written in one pixel component area of the mask data storing memory 2', so that a plurality of pictures will never be written at the same position of the video VRAM 4 if the number of a motion picture input has been defined exclusively.

Therefore, according to the present embodiment, it is possible to display a motion picture window by merely drawing in the mask data storing memory the number data of the motion picture input to be displayed, in the manner similar to that of the conventional graphics drawing. As a result, there is an effect that the operator can handle the window display without being conscious about the dynamic window.

Claims

1. A video picture display device, comprising:

   means (1) for inputting pixel data corresponding to each pixel of a video picture structured by a predetermined number of pixels;

   a bit map memory (4) for storing said inputted pixel data;

   means (5, 6) for displaying said video picture on a display screen (70) of display means (7) within a computer main body (100) based on pixel data stored in said bit map memory (4); and

   a masking memory (2) for masking pixel data according to the shape of a display area of said video picture displayed on said display screen (70), characterized in that:

   said masking memory (2) has a bit number equal to or less than said predetermined number of inputted pixel data,

   said masking memory (2) is provided separate from said bit memory (4), and

   said video picture display device (110) further includes write control means (3), disposed between said pixel data input means (1) and said bit map memory (4) and connected with said masking memory (2), for reading mask data corresponding to pixel data from said masking memory (2) in response to input pixel data from said pixel data input means and for controlling, without reading said bit map memory, to determine whether said pixel data is to be written in said bit map memory or not.

2. A video picture display device according to Claim 1, characterized in that:

   said mask data (200 - 205) are being divided for each plurality of scanning lines of said video picture within said masking memory (2),

   each of said divided mask data is added with coordinates data (240 - 245) for expressing a write starting address to said bit map memory of a plurality of pixel data that structure scanning lines corresponding to said divided mask data, and

   said write control means (3) determines an address within said bit map memory of pixel data to be written in said bit map memory, based on said coordinates data.

3. A video picture display device according to Claim 2, characterized in that:
within said masking memory (2), said mask data is divided into a scanning line direction and a subscanning line direction of said video picture respectively so that said mask data is divided into a plurality of mask groups (20 - 1 to 20 - 4),
each of said divided groups is added with coordinates data (24 - 1 to 24 - 4) for expressing write starting address to said bit map memory of a plurality of pixel data that structure scanning lines belonging to each of said divided mask group, and
said write control means (3) determines an address within said bit map memory of pixel data to be written in said bit map memory, based on said coordinates data.

4. A video picture display device according to Claim 2 or 3, characterized in that each of said coordinates data includes direction data (250 - 255) for showing in which direction of a forward direction or a backward direction a column structured by a plurality of pixel data corresponding to each of said coordinates data is written within said bit map memory.

5. A video picture display device according to any one of Claims 2 to 4, characterized in that said coordinates data can be rewritten from said video picture display device side.

6. A video picture display device according to any one of Claims 1 to 3, including at least two of said masking memories (25 and 26), characterized in that
said write control means (3) includes:
means (41) for instructing one of said at least two masking memories as a masking memory to be used;
synchronization timing generating means (42) for generating a timing signal synchronous with a vertical synchronizing signal of said video picture; and
means (32) for selecting one from said at least two masking memories in response to an instruction from said instructing means during a generation of said timing signal,
an updating of said mask data being carried out for an un-selected masking memory of said at least two masking memories.

7. A video picture display device according to Claim 6, characterized in that said write control means (3) further includes means (48) for changing over said input picture data with data of a specific color during a generation of a timing signal from said synchronization timing signal generating means (42) in response to an instruction from said instructing means, and
said selecting means (32) selects one from said at least two masking memories in response to said instructing means during a generation of a next timing signal.

8. A video picture display device according to Claim 1, further including:
means (5) for reading pixel data stored in said bit map memory (4);
picture change-over means (6) disposed between said bit map memory (4) and said display means (7), for changing over between picture data read out from said bit map memory and graphics data from graphics display means (8) within said computer main body (100) and sending changed data to said display means; and
a keying data memory (9) for storing keying data for changing over pictures of a bit number corresponding to a number of pixels that structure a display screen (70) of said display means to be used by said picture change-over means (6),
said masking memory (2) and said keying data memory (9) being disposed within the same memory.

9. A video picture display device according to Claim 2 or 3, wherein, when a compressed picture of said input video picture is to be displayed on said display screen (70), said write control means (3) further includes:
first decision means (51) for determining at least one pixel data to be allocated from a plurality of pixel data for structuring one scanning line of said input video picture to each of a plurality of pixels that structure one scanning line of said compressed picture, by using an oblique line generating algorithm;
first selecting means (52) for selecting one from at least one pixel data allocated by said first decision means (51) to each of a plurality of pixels that structure one scanning line of said compressed picture;
second decision means (53) for determining at least one scanning line to be allocated from a plurality of scanning lines for structuring said input video picture to each of a plurality of scanning lines that structure said compressed picture, by using an oblique line generating algorithm; and
second selecting means (54) for selecting one from at least one scanning line allocated by said second decision means (53) to each of a plurality of scanning lines that structure said

compressed picture, and characterized in that said masking memory (2) stores data necessary for the processing of said first and second decision means and said first and second selecting means as a part of said coordinates data (24), and said writing means (3) selectively writes in said bit map memory (4) said selected pixel data by said selected scanning line based on mask data within said masking memory (2).

10. A video picture display device according to Claim 2 or 3, wherein, when a compressed picture of said input video picture is to be displayed on said display screen (70), said write control means (3) further includes:

first decision means (51) for determining at least one pixel data to be allocated from a plurality of data for structuring one scanning line of said input video picture to each of a plurality of pixels that structure one scanning line of said compressed picture, by using an oblique line generating algorithm;

first averaging means (55) for averaging at least one pixel data allocated by said first decision means (51) to each of a plurality of pixels that structure one scanning line of said compressed picture;

second decision means (53) for determining at least one scanning line to be allocated from a plurality of scanning lines for structuring said input video picture to each of a plurality of scanning lines that structure said compressed picture, by using an oblique line generating algorithm; and

second averaging means (55) for averaging at least one scanning line allocated by said second decision means (53) to each of a plurality of scanning lines that structure said compressed picture, and characterized in that

said masking memory (2) stores data necessary for the processing of said first and second decision means and said first and second averaging means as a part of said coordinates data (24), and

said writing means (3) selectively writes in said bit map memory (4) said averaged pixel data by said averaged scanning line based on mask data within said masking memory (2).

11. A video picture display device according to Claim 10, characterized in that said first averaging means (55) includes first shifting means (551) for obtaining a power of 2 for each value of pixel data that has been allocated by said first decision means (51);

first adding means (552 - 554) for adding pixel data values that have been processed by said first shifting means (551); and

second shifting means (555) for obtaining a minus power of 2 for said added pixel data value.

12. A video picture display device according to Claim 11, characterized in that said second averaging means (56) includes third shifting means (561) for obtaining 2 to a power of 2 for each pixel data of each pixel data group corresponding to scanning line groups allocated by said second decision means (53);

second adding means (562 -564) for adding pixel data values that have been processed by said first shifting means (551); and

fourth shifting means (565) for obtaining a minus power of 2 for said added pixel data value.

13. A video picture display device, comprising:

means (12 - 14) for inputting pixel data corresponding to each pixel of a video picture structured by a predetermined number of pixels;

a bit map memory (4'), having a bit number corresponding to a number of pixels that structure a display screen of display means (7), for storing said inputted pixel data;

means (5, 6) for displaying on a display screen (70) of said display means (7) based on pixel data stored in said bit map memory (4'); and

a masking memory (2') for masking pixel data according to the shape of a display area of said video picture displayed on said display screen, characterized in that:

said input means (12 - 14) inputs a plurality of video pictures and said plurality of input video pictures are given different numbers,

said masking memory (2') has mask data of a plurality of bits for each of a plurality of pixels that structure said display screen and assigns a number of an input video picture to be displayed on said pixel with said plurality of mask data,

said masking memory (2') is provided separately from said bit map memory (4'), and

said video picture display device further includes write control means (3) write control means (3), disposed between said pixel data input means (12 - 14) and said bit map memory (4') and connected with said masking memory (2'), for reading mask data of a plurality of bits corresponding to pixel data from said masking memory (2') in response to input pixel data from said pixel data input means and a video picture number, for comparing a value of said plurality of bits that have been read with

said video picture number, and writing in said bit map memory said pixel data when both values coincide with each other.

14. A method for controlling a video picture display for inputting motion picture data and displaying said motion picture data by using a bit map memory, characterized in that said method includes the processing of:

storing write mask data of said motion picture data;

reading said write mask data corresponding to said motion picture data;

assigning a write position of a picture corresponding to said motion picture data; and

determining whether said motion picture data should be written in said bit map memory or not according to the contents of said write mask data that have been read out.

15. A method for controlling a video picture display for inputting motion picture data and displaying said motion picture data by using a bit map memory, characterized in that said method includes the processing of:

storing coordinates data for writing said motion picture data for each horizontal scanning;

generating at least one dimensional write address;

reading said coordinates data to be written prior to the writing for each horizontal scanning; and

setting said coordinates data that have been read in an initial address of said write address.

16. A method for controlling a video picture display for inputting motion picture data and displaying said motion picture data by using a bit map memory, characterized in that said method includes the processing of:

storing at least two sets of write mask data;

generating a timing signal synchronous with a vertical synchronization signal of said motion picture data;

instructing a change-over of said mask data;

controlling a change-over of said write mask data according to said timing signal and said instruction; and

generating a status display flag for showing a status of said change-over.

17. A method for controlling a video picture display according to Claim 16, further including the processing of forcibly changing over said motion picture data to data of a special color.

18. A method for controlling a video picture display for inputting a plurality of motion picture data and displaying said motion picture data by using a bit map memory, characterized in that said method includes the processing of:

storing assigned plurality of bits corresponding to each bit map of said bit map memory;

exclusively defining own picture input number corresponding to each one of said plurality of motion picture data;

detecting a coincidence between said picture input number and the contents of said assigned plurality of bits for each bit map; and

writing only said motion picture data of which coincidence has been detected, in said bit map memory.

19. A method for controlling a display of a video picture for displaying a compressed picture of a video picture written in a bit map memory (4) within a predetermined area on a display screen (70) of display means within a computer main body (100), comprising the steps of:

inputting a video picture structured by a first predetermined number of pixels for each pixel data;

determining at least one pixel data to be allocated from a plurality of pixel data for structuring one scanning line of said input video picture to each of a plurality of pixels that structure one scanning line of said compressed picture, by using an oblique line generating algorithm;

selecting one from at least one pixel data allocated to each of a plurality of pixels that structure one scanning line of said compressed picture;

determining at least one scanning line to be allocated from a plurality of scanning lines for structuring said input video picture to each of a plurality of scanning lines that structure said compressed picture, by using an oblique line generating algorithm;

selecting one from at said least one scanning line allocated to each of a plurality of scanning lines that structure said compressed picture; and

writing in said bit map memory (4) said selected pixel data by said selected scanning line.

20. A method for controlling a display of a video picture for displaying a compressed picture of a video picture written in a bit map memory (4)

within a predetermined area on a display screen (70) of display means within a computer main body (100), comprising the steps of:

inputting a video picture structured by a first predetermined number of pixels for each pixel data;

determining at least one pixel data to be allocated from a plurality of pixel data for structuring one scanning line of said input video picture to each of a plurality of pixels that structure one scanning line of said compressed picture, by using an oblique line generating algorithm;

averaging one pixel data from said at least one pixel data allocated to each of a plurality of pixels that structure one scanning line of said compressed picture;

determining at least one scanning line to be allocated from a plurality of scanning lines for structuring said input video picture to each of a plurality of scanning lines that structure said compressed picture, by using an oblique line generating algorithm;

averaging said at least one scanning line allocated to each of a plurality of scanning lines for structuring said compressed picture; and

writing in said bit map memory (4) said averaged pixel data by said averaged scanning line.

21. A method for controlling a display of a video picture according to Claim 19, further including a masking memory (2) for masking pixel data according to the shape of the display area of said video picture to be displayed on said display screen (70), characterized in that:

said selected pixel data in said selected scanning line is selectively written in said bit map memory (4) based on mask data within said masking memory (2).

22. A method for controlling a display of a video picture according to Claim 20, further including a masking memory (2) for masking pixel data according to the shape of a display area of said video picture to be displayed on said display screen (70), characterized in that:

said masking memory (2) has mask data of a bit number equal to or less than a predetermined number of said inputted pixel data;

said masking memory (2) is provided separate from said bit map memory (4); and

said averaged pixel data in said averaged scanning line is selectively written in said bit map memory (4) based on mask data within said masking memory (2).

23. A method for controlling a display of a video picture according to Claim 19 or 21, characterized in that said step of selecting at least one pixel data comprises the following steps of:

setting a quotient obtained by dividing a number of pixels for structuring said input video picture by a number of pixels of a compressed picture on said display screen as the number of basic pixel data of said selected pixel data;

adding remainders of said division for each pixel of said compressed picture (step 101);

comparing said added remainder with 1 (step 102); and

when a result of said comparison is at least 1, setting the number of said selected pixel data for a corresponding pixel of the compressed picture to said basic pixel data + 1 (step 104).

24. A method for controlling a display of a video picture according to Claim 20 or 22, characterized in that said step of selecting at least one pixel data comprises the following steps of:

setting a quotient obtained by dividing a number of pixels for structuring said input video picture by a number of pixels of a compressed picture on said display screen as the number of basic pixel data of said averaged pixel data;

adding remainders of said division for each pixel of said compressed picture (step 101);

comparing said added remainder with 1 (step 102); and

when a result of said comparison is at least 1, setting the number of said averaged pixel data for a corresponding pixel of the compressed picture to said basic pixel data + 1 (step 104).

25. A method for controlling a display of a video picture according to Claim 19 or 21, characterized in that said step of selecting at least one pixel data comprises the following steps of:

setting a quotient obtained by dividing a number of pixels for structuring said input video picture by a number of pixels of a compressed picture on said display screen as the number of basic pixel data of said selected pixel data;

substituting - (the number of pixels of a compressed picture on said display screen) as an initial value of a value A (step 110);

adding to said value A value R which is a result of a remainder of said division multiplied by a number of pixels of a compressed picture on said display screen, to obtain a new value A (step 111);

comparing said value A with 0 (step 112); and

when a result of said comparison is at least 0, setting the number of said selected pixel data for a corresponding pixel of the compressed picture to said basic pixel data + 1 (step 114).

26. A method for controlling a display of a video picture according to Claim 20 or 22, characterized in that said step of selecting at least one pixel data comprises the following steps of:

setting a quotient obtained by dividing a number of pixels for structuring said input video picture by a number of pixels of a compressed picture on said display screen as the number of basic pixel data of said selected pixel data;

substituting - (the number of pixels of a compressed picture on said display screen) as an initial value of a value A (step 110);

adding to said value A value R which is a result of a remainder of said division multiplied by a number of pixels of a compressed picture on said display screen, to obtain a new value A (step 111);

comparing said value A with 0 (step 112); and

when a result of said comparison is at least 0, setting the number of said selected pixel data for a corresponding pixel of the compressed picture to said basic pixel data + 1 (step 114).

FIG. 1

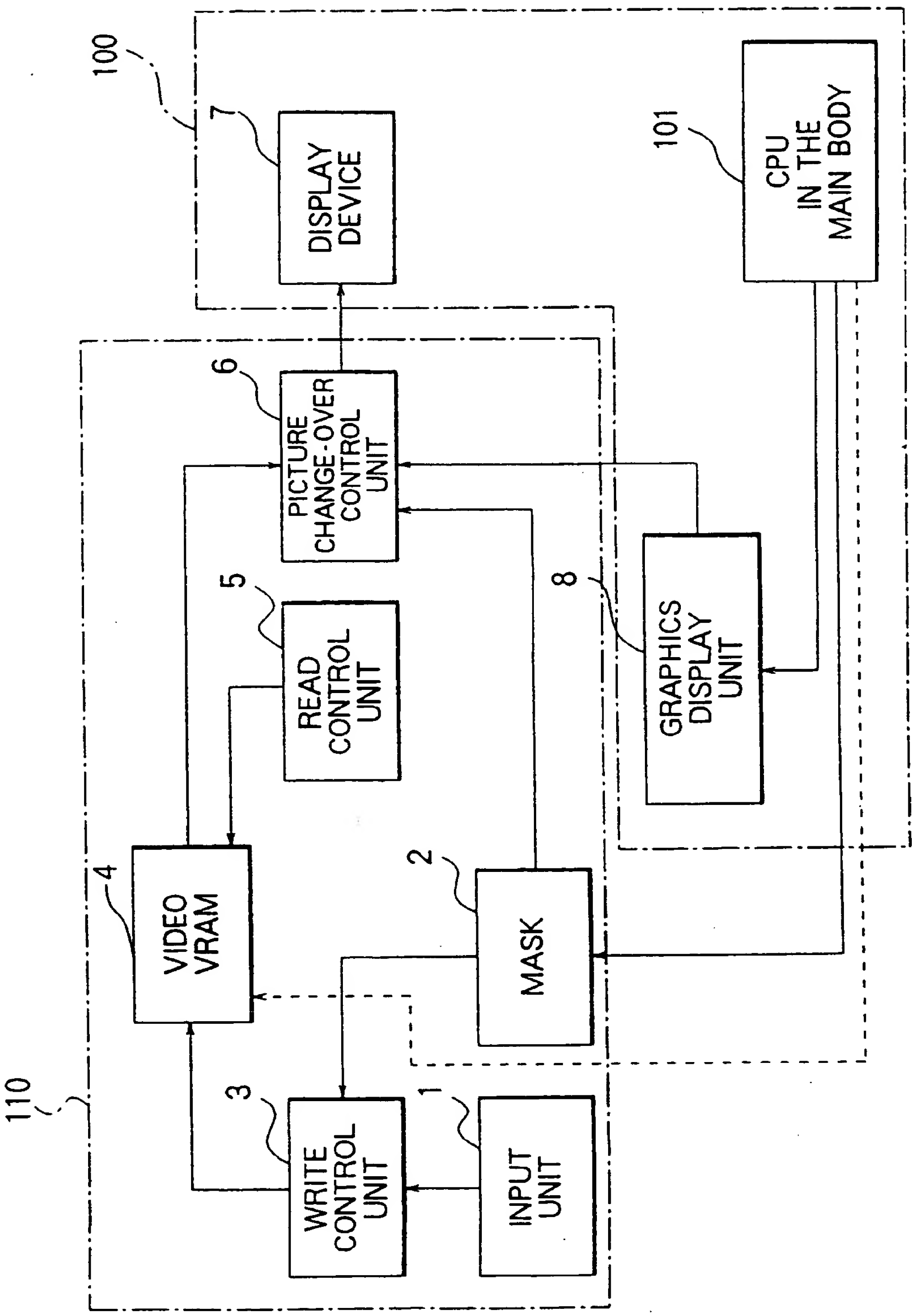

100
7
DISPLAY DEVICE
101
CPU IN THE MAIN BODY
6
PICTURE CHANGE-OVER CONTROL UNIT
5
READ CONTROL UNIT
8
GRAPHICS DISPLAY UNIT
4
VIDEO VRAM
2
MASK
110
3
WRITE CONTROL UNIT
1
INPUT UNIT

FIG. 2

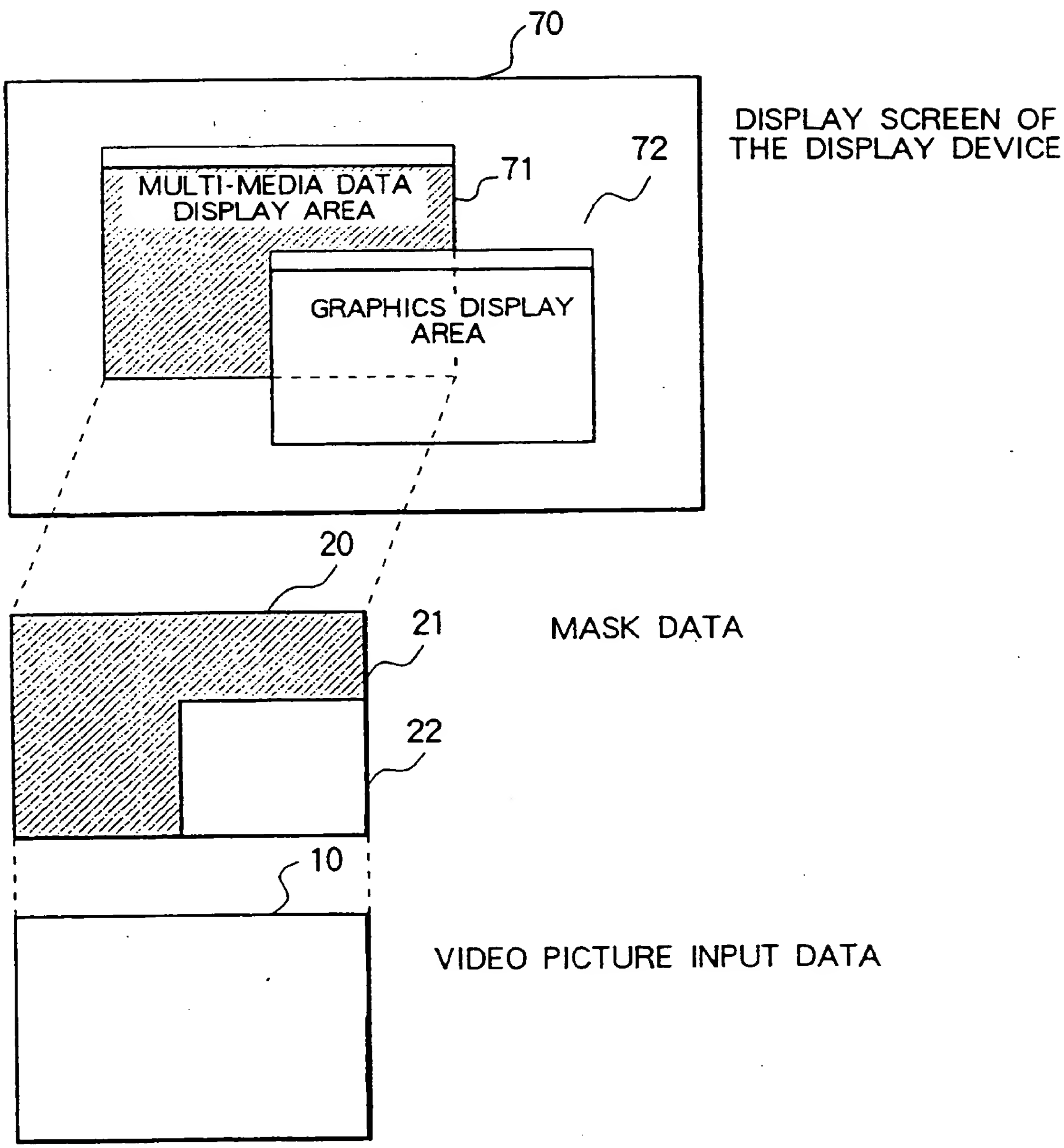

70
71
72
MULTI-MEDIA DATA DISPLAY AREA
GRAPHICS DISPLAY AREA
DISPLAY SCREEN OF THE DISPLAY DEVICE
20
21
22
MASK DATA
10
VIDEO PICTURE INPUT DATA

FIG. 3

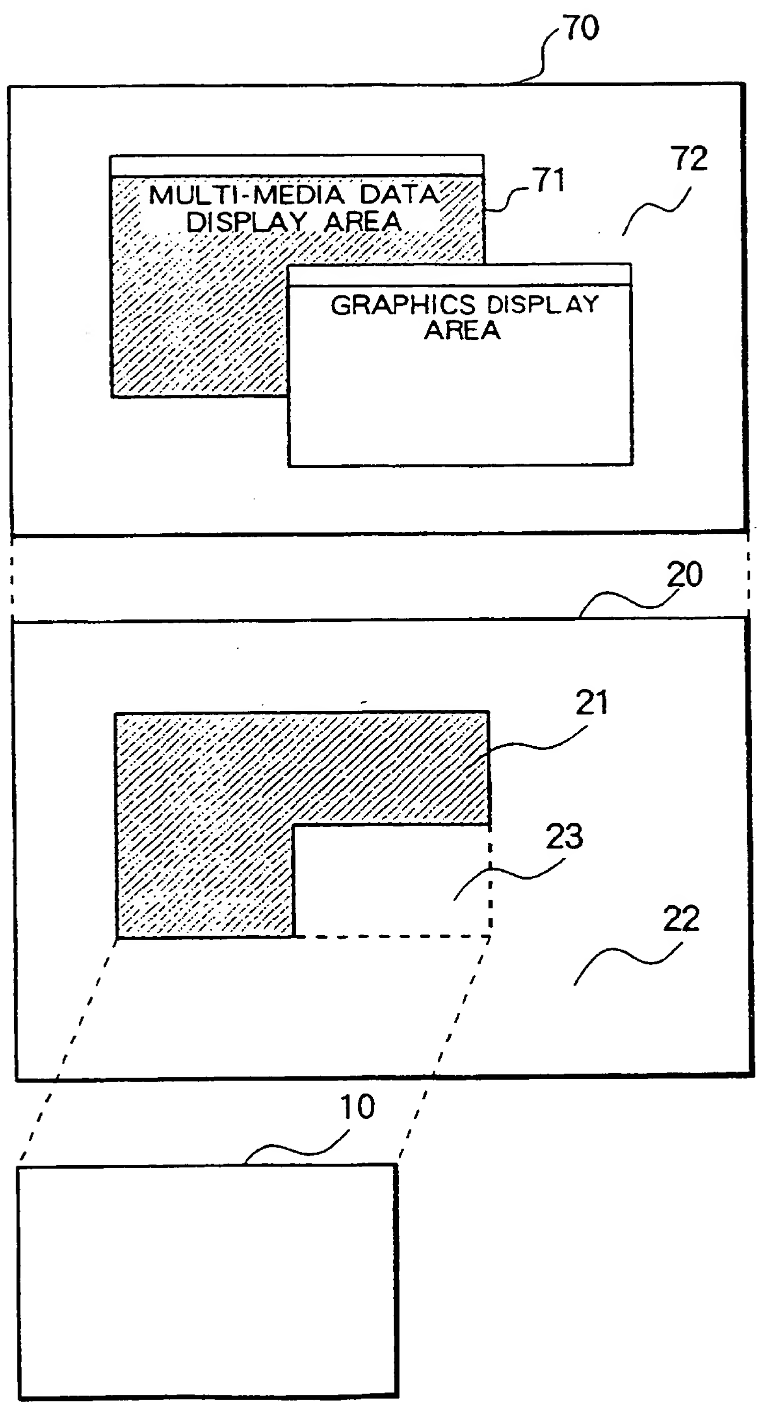

70
72
71
MULTI-MEDIA DATA DISPLAY AREA
GRAPHICS DISPLAY AREA
20
21
23
22
10

FIG. 4

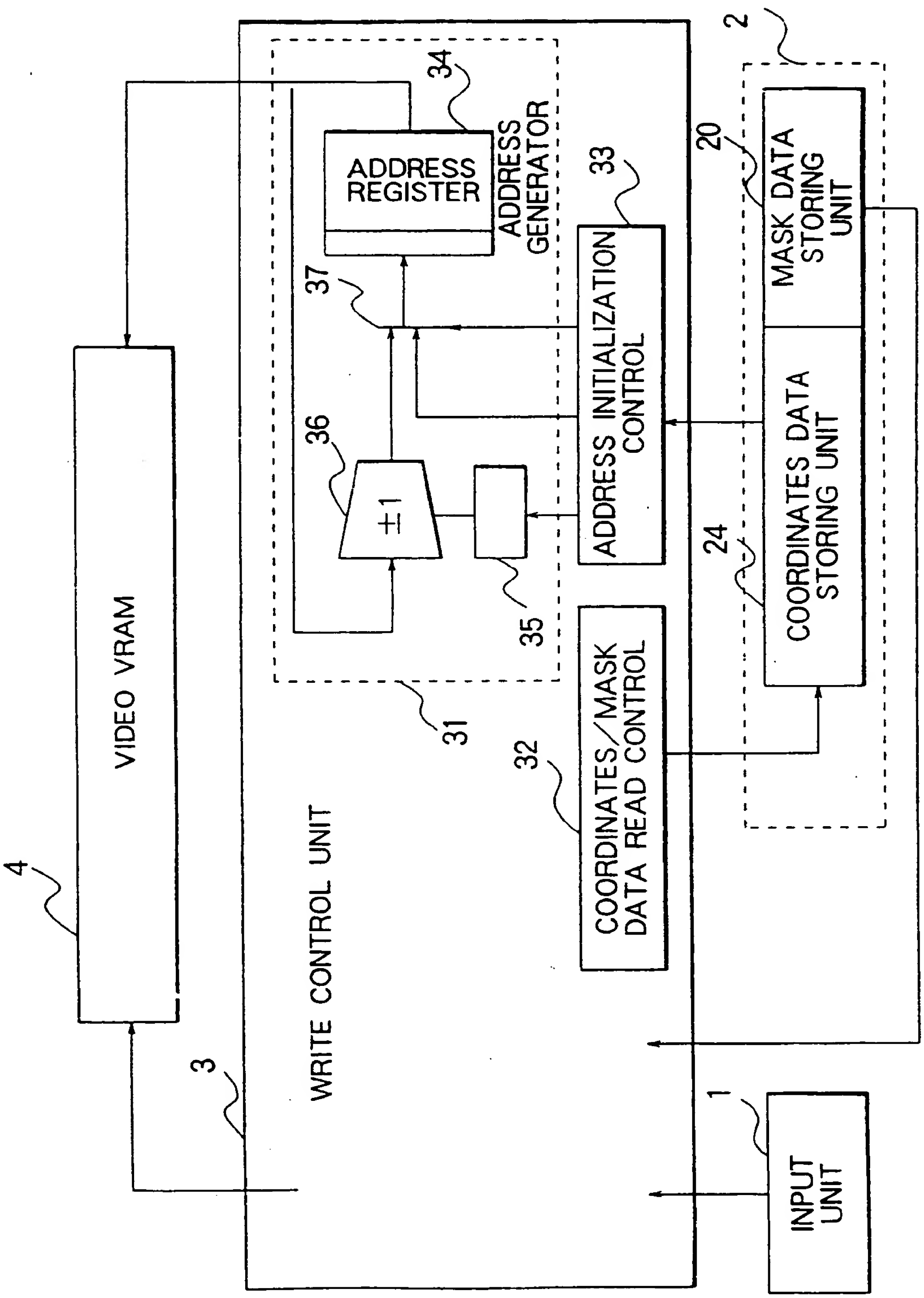

VIDEO VRAM
4
WRITE CONTROL UNIT
3
ADDRESS REGISTER
34
ADDRESS GENERATOR
37
36
±1
35
31
ADDRESS INITIALIZATION CONTROL
33
COORDINATES/MASK DATA READ CONTROL
32
MASK DATA STORING UNIT
20
COORDINATES DATA STORING UNIT
24
2
INPUT UNIT
1

FIG. 5

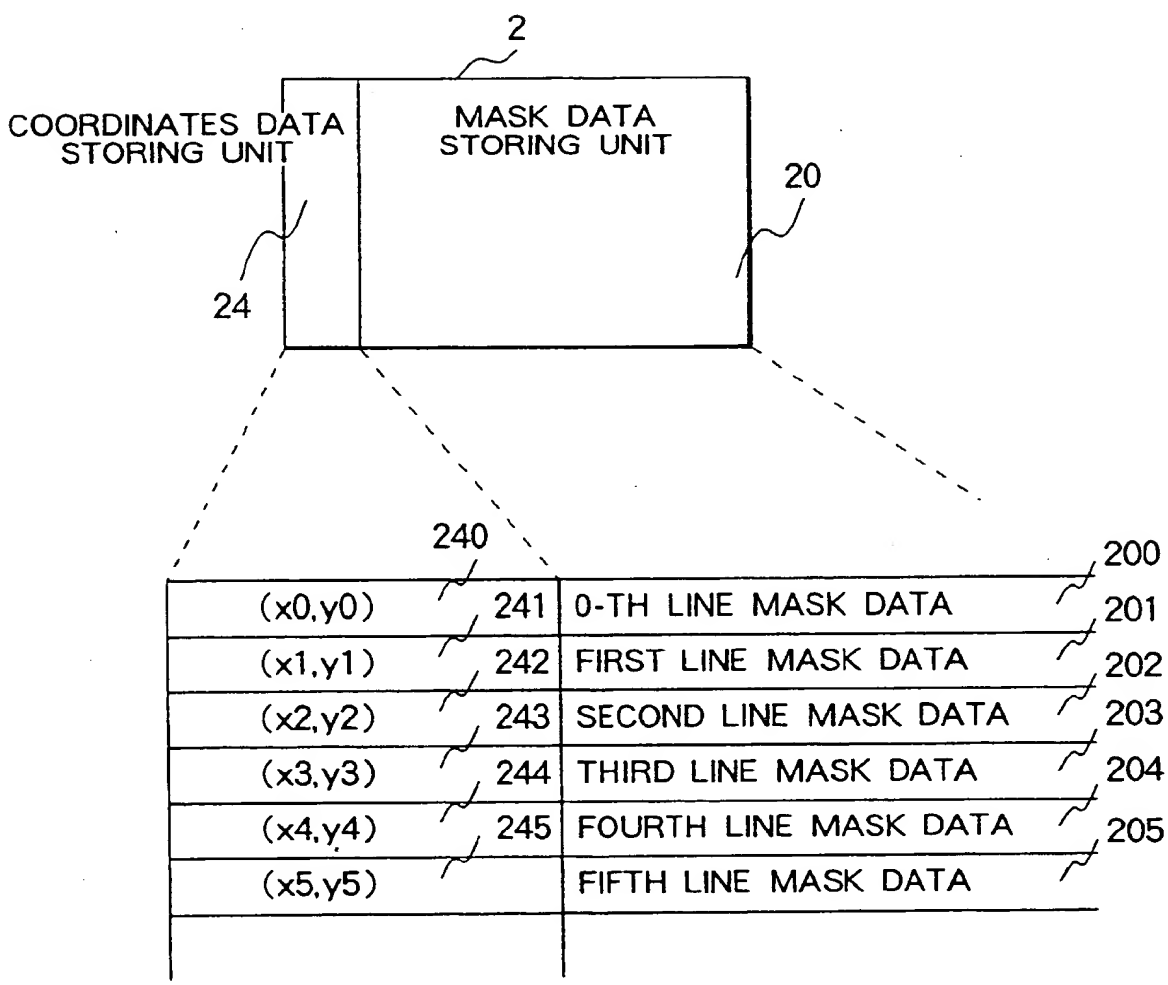

2
COORDINATES DATA STORING UNIT
MASK DATA STORING UNIT
20
24
240
200
(x0,y0)
241
0-TH LINE MASK DATA
201
(x1,y1)
242
FIRST LINE MASK DATA
202
(x2,y2)
243
SECOND LINE MASK DATA
203
(x3,y3)
244
THIRD LINE MASK DATA
204
(x4,y4)
245
FOURTH LINE MASK DATA
205
(x5,y5)
FIFTH LINE MASK DATA

FIG. 6

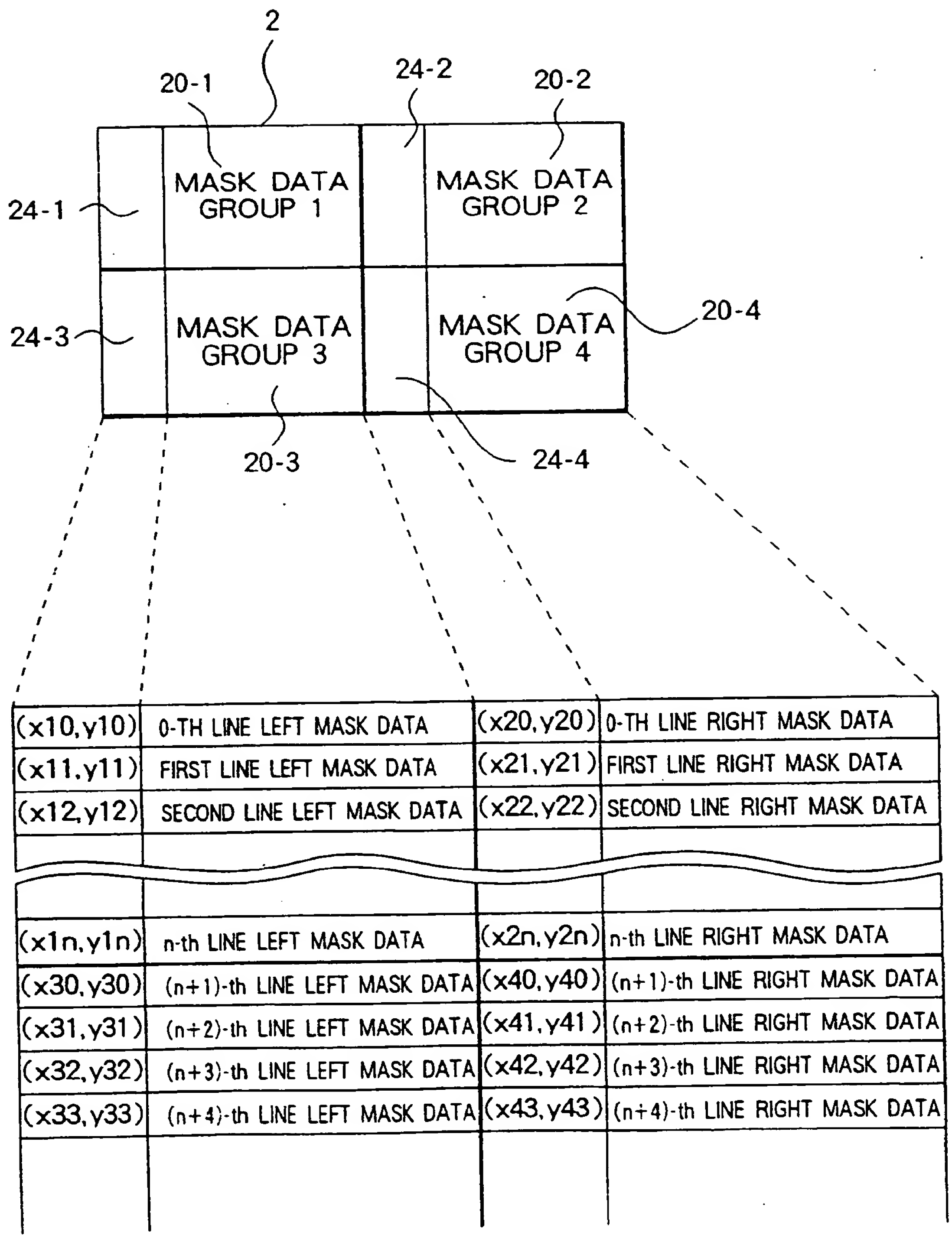

2
20-1
24-2
20-2
MASK DATA GROUP 1
MASK DATA GROUP 2
24-1
MASK DATA GROUP 3
MASK DATA GROUP 4
24-3
20-4
20-3
24-4
(x10,y10) 0-TH LINE LEFT MASK DATA
(x20,y20) 0-TH LINE RIGHT MASK DATA
(x11,y11) FIRST LINE LEFT MASK DATA
(x21,y21) FIRST LINE RIGHT MASK DATA
(x12,y12) SECOND LINE LEFT MASK DATA
(x22,y22) SECOND LINE RIGHT MASK DATA
(x1n,y1n) n-th LINE LEFT MASK DATA
(x2n,y2n) n-th LINE RIGHT MASK DATA
(x30,y30) (n+1)-th LINE LEFT MASK DATA
(x40,y40) (n+1)-th LINE RIGHT MASK DATA
(x31,y31) (n+2)-th LINE LEFT MASK DATA
(x41,y41) (n+2)-th LINE RIGHT MASK DATA
(x32,y32) (n+3)-th LINE LEFT MASK DATA
(x42,y42) (n+3)-th LINE RIGHT MASK DATA
(x33,y33) (n+4)-th LINE LEFT MASK DATA
(x43,y43) (n+4)-th LINE RIGHT MASK DATA

FIG. 7

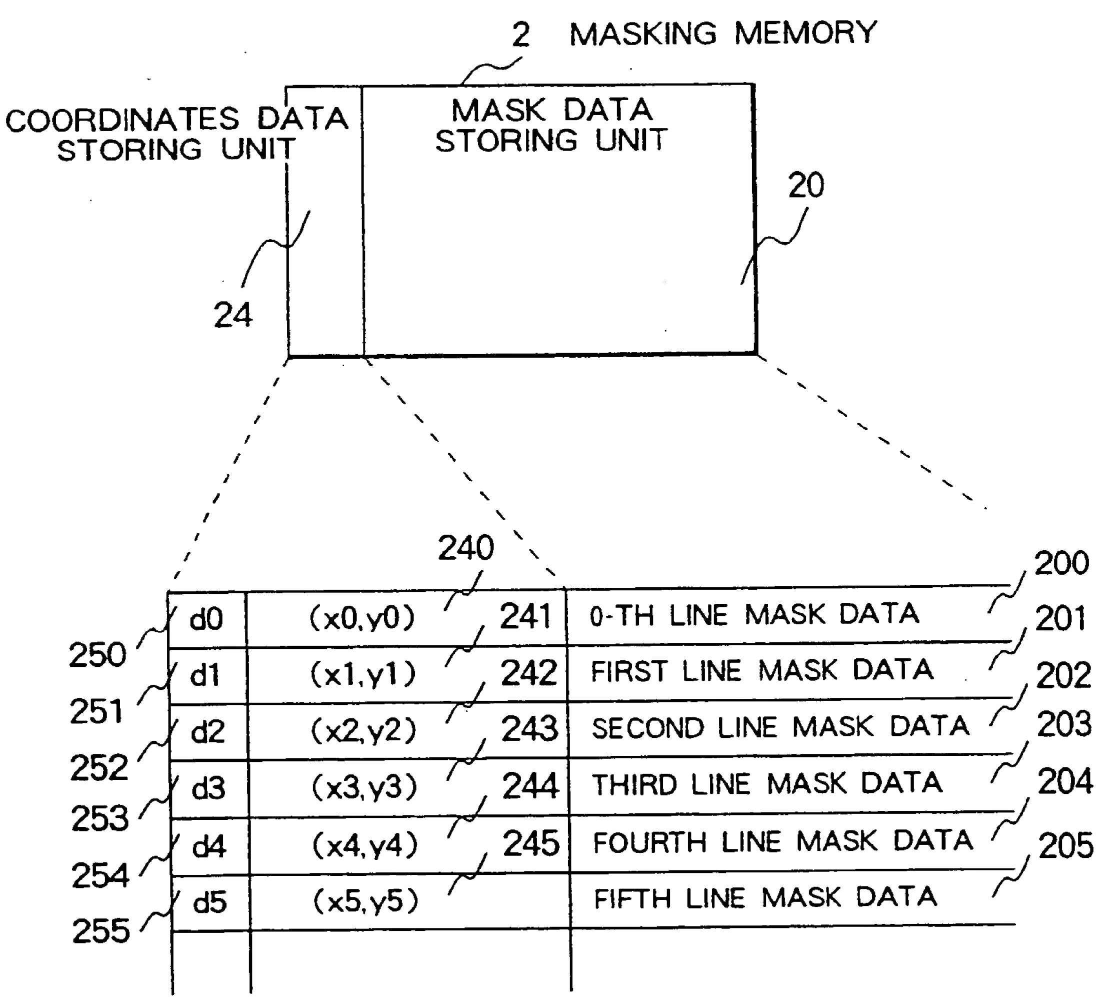

2 MASKING MEMORY
COORDINATES DATA STORING UNIT
MASK DATA STORING UNIT
20
24
240
200
d0
(x0,y0)
241
0-TH LINE MASK DATA
201
250
d1
(x1,y1)
242
FIRST LINE MASK DATA
202
251
d2
(x2,y2)
243
SECOND LINE MASK DATA
203
252
d3
(x3,y3)
244
THIRD LINE MASK DATA
204
253
d4
(x4,y4)
245
FOURTH LINE MASK DATA
205
254
d5
(x5,y5)
FIFTH LINE MASK DATA
255

FIG. 8

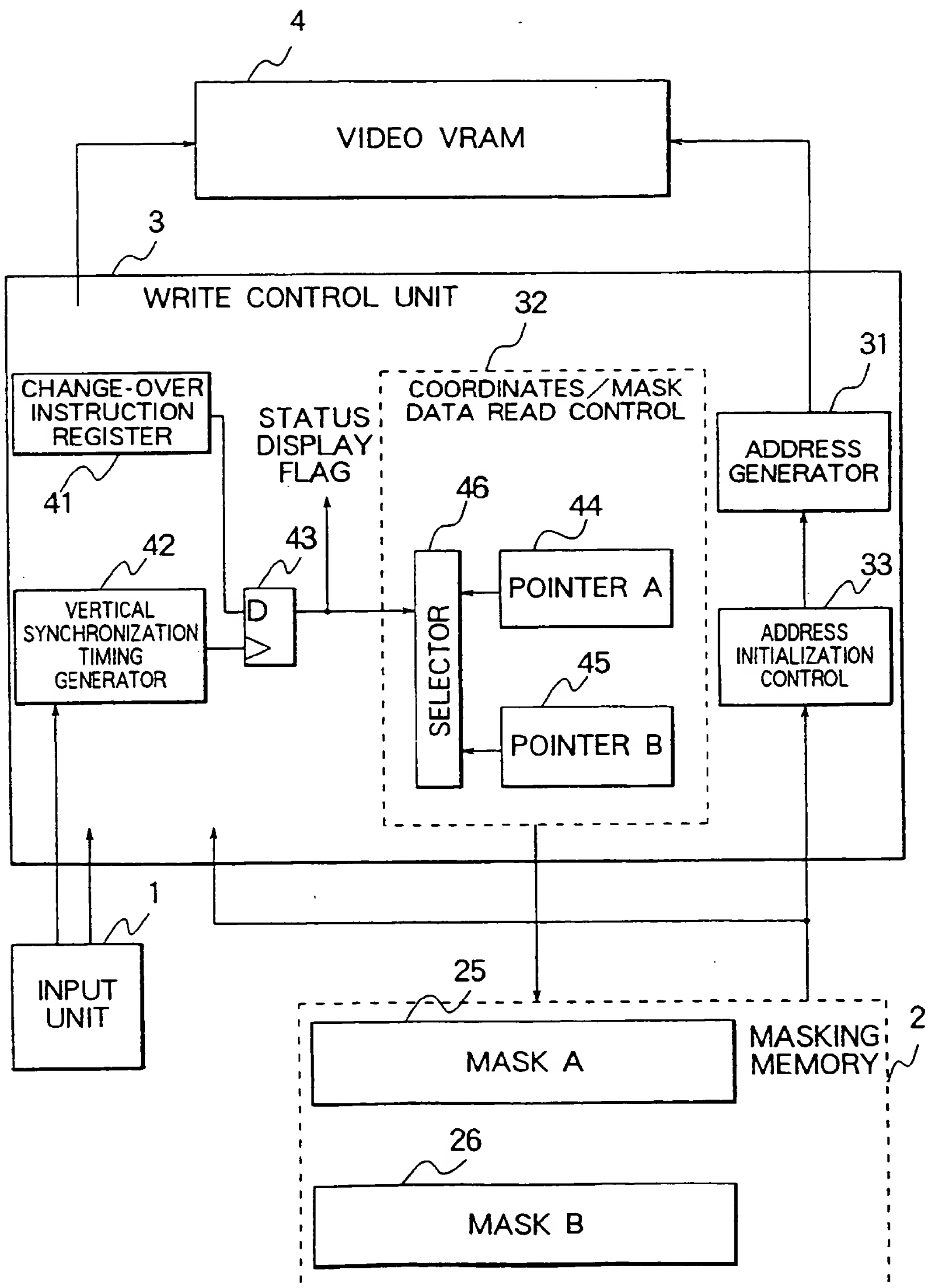

4
VIDEO VRAM
3
WRITE CONTROL UNIT
32
COORDINATES／MASK DATA READ CONTROL
31
CHANGE-OVER INSTRUCTION REGISTER
STATUS DISPLAY FLAG
ADDRESS GENERATOR
41
46
44
42
43
33
VERTICAL SYNCHRONIZATION TIMING GENERATOR
D
POINTER A
ADDRESS INITIALIZATION CONTROL
SELECTOR
45
POINTER B
1
INPUT UNIT
25
MASK A
MASKING MEMORY
2
26
MASK B

FIG. 9

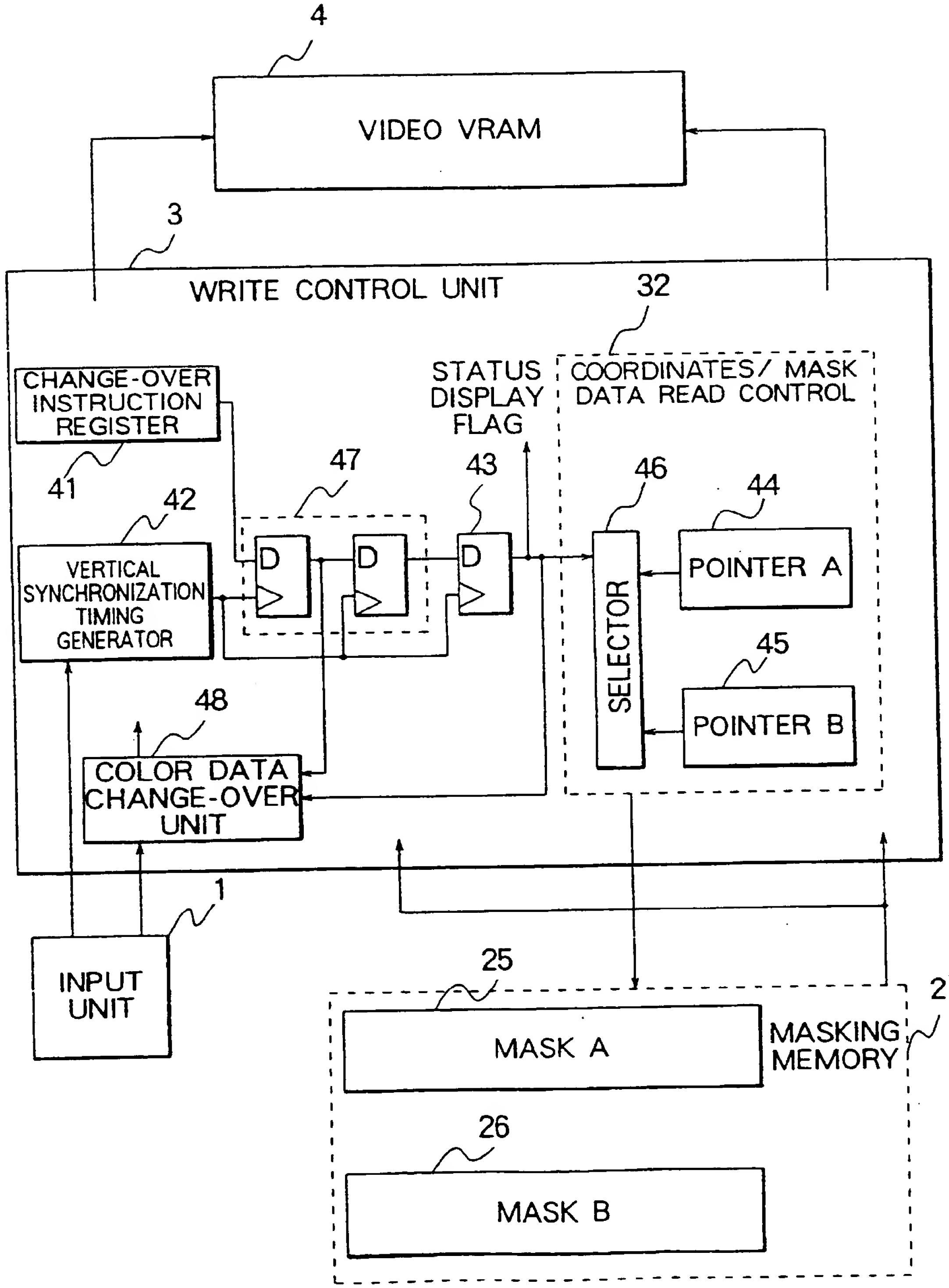

4
VIDEO VRAM
3
WRITE CONTROL UNIT
32
CHANGE-OVER INSTRUCTION REGISTER
41
STATUS DISPLAY FLAG
COORDINATES/ MASK DATA READ CONTROL
47
43
46
44
42
VERTICAL SYNCHRONIZATION TIMING GENERATOR
D
D
D
SELECTOR
POINTER A
45
POINTER B
48
COLOR DATA CHANGE-OVER UNIT
1
INPUT UNIT
25
2
MASK A
MASKING MEMORY
26
MASK B

FIG. 10

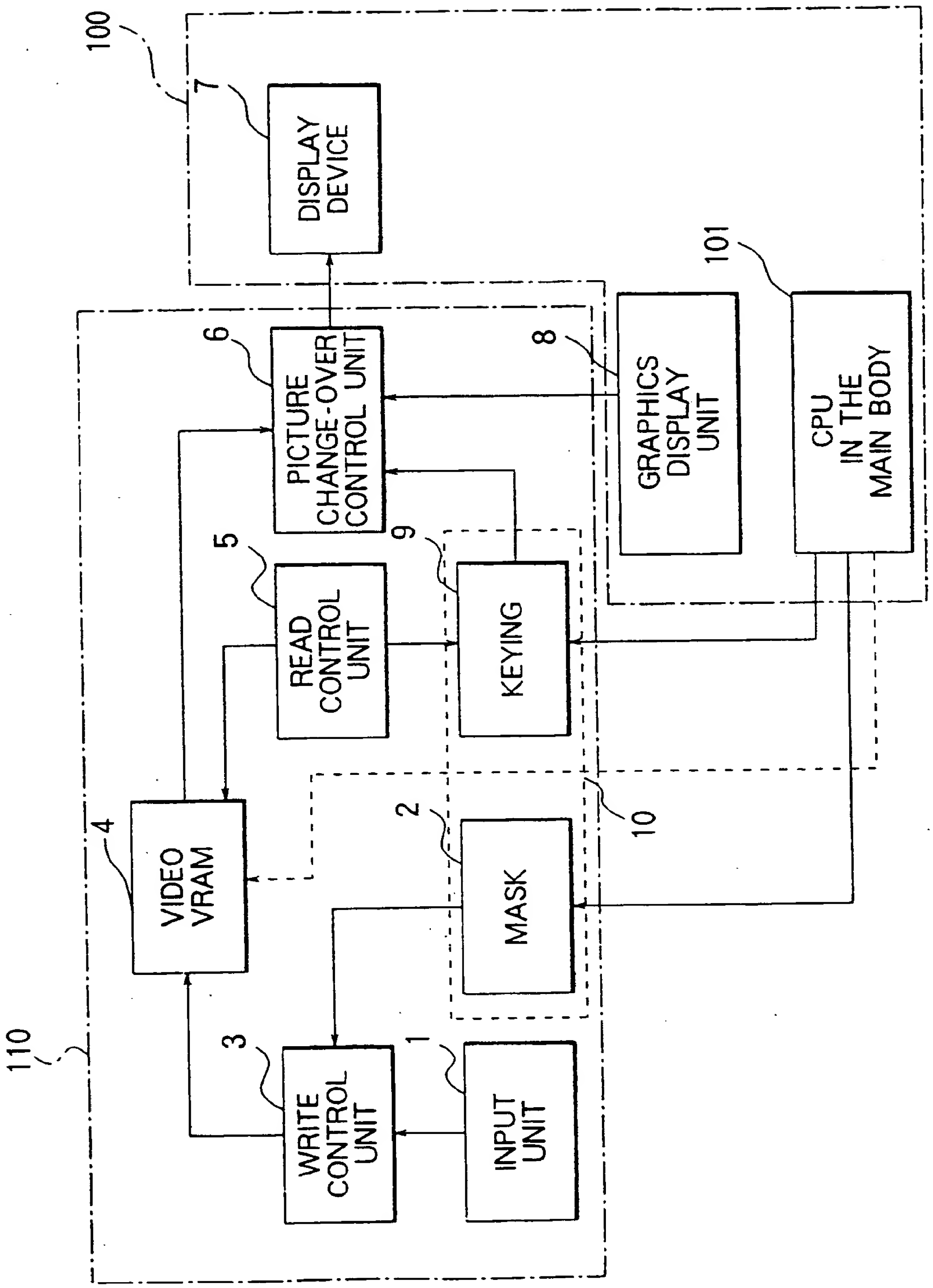

100
7
DISPLAY DEVICE
101
6
PICTURE CHANGE-OVER CONTROL UNIT
8
GRAPHICS DISPLAY UNIT
CPU IN THE MAIN BODY
5
9
READ CONTROL UNIT
KEYING
4
VIDEO VRAM
2
MASK
10
110
3
1
WRITE CONTROL UNIT
INPUT UNIT

FIG. 11

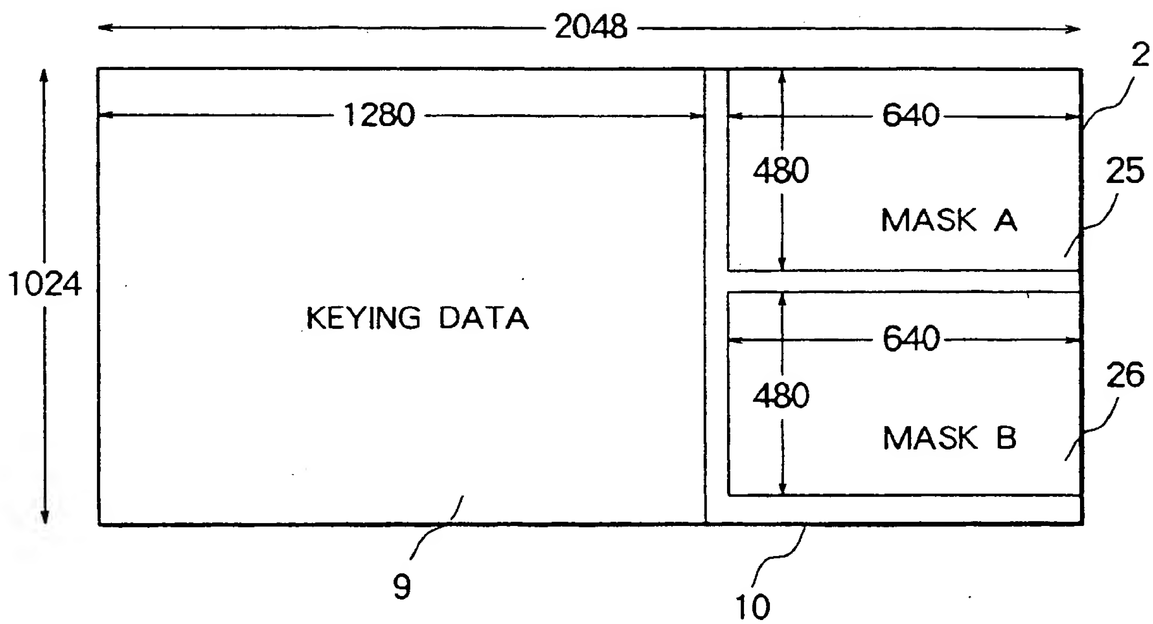

2048
1280
640
480
MASK A
640
480
MASK B
1024
KEYING DATA
2
25
26
9
10

FIG. 12

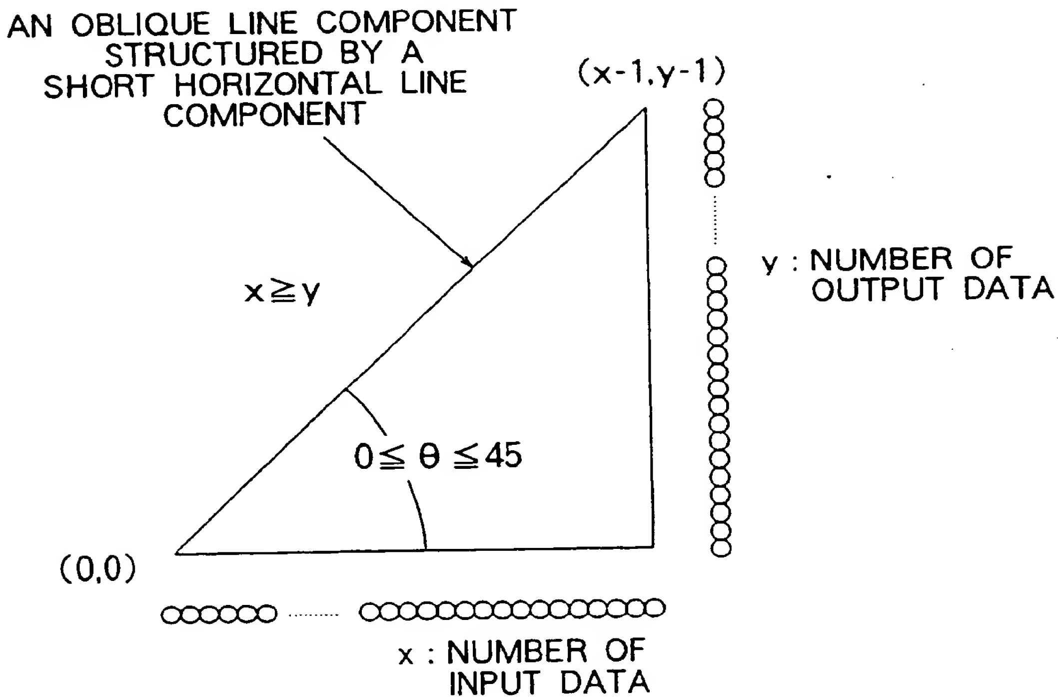

AN OBLIQUE LINE COMPONENT STRUCTURED BY A SHORT HORIZONTAL LINE COMPONENT
(x-1,y-1)
x≧y
0≦ θ ≦45
(0,0)
y : NUMBER OF OUTPUT DATA
x : NUMBER OF INPUT DATA

FIG. 13

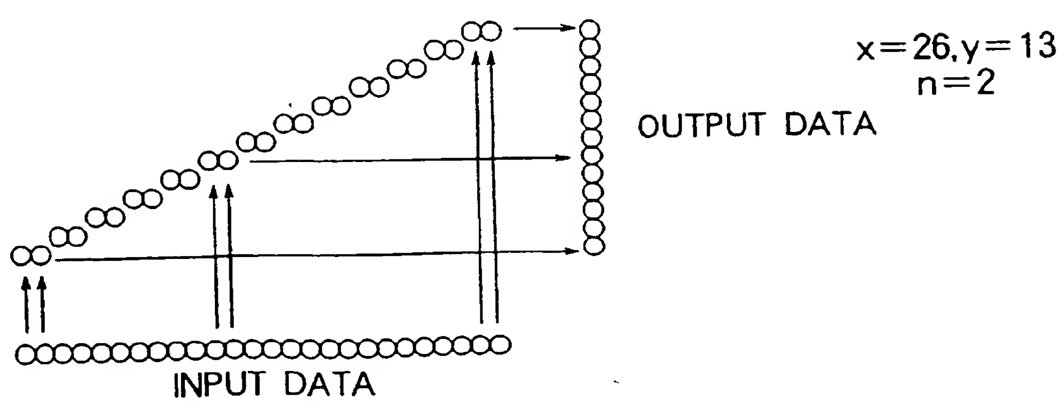

x=26,y=13
n=2
OUTPUT DATA
INPUT DATA

FIG. 14

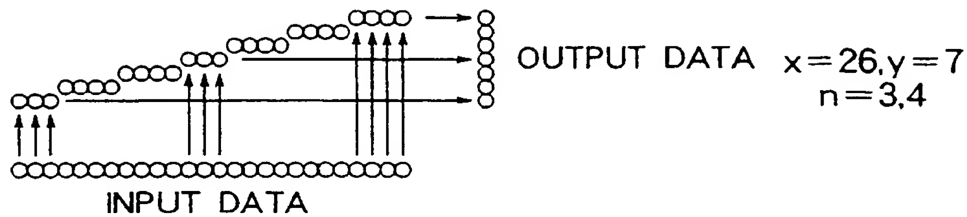

OUTPUT DATA
x=26, y=7
n=3,4
INPUT DATA

FIG. 15

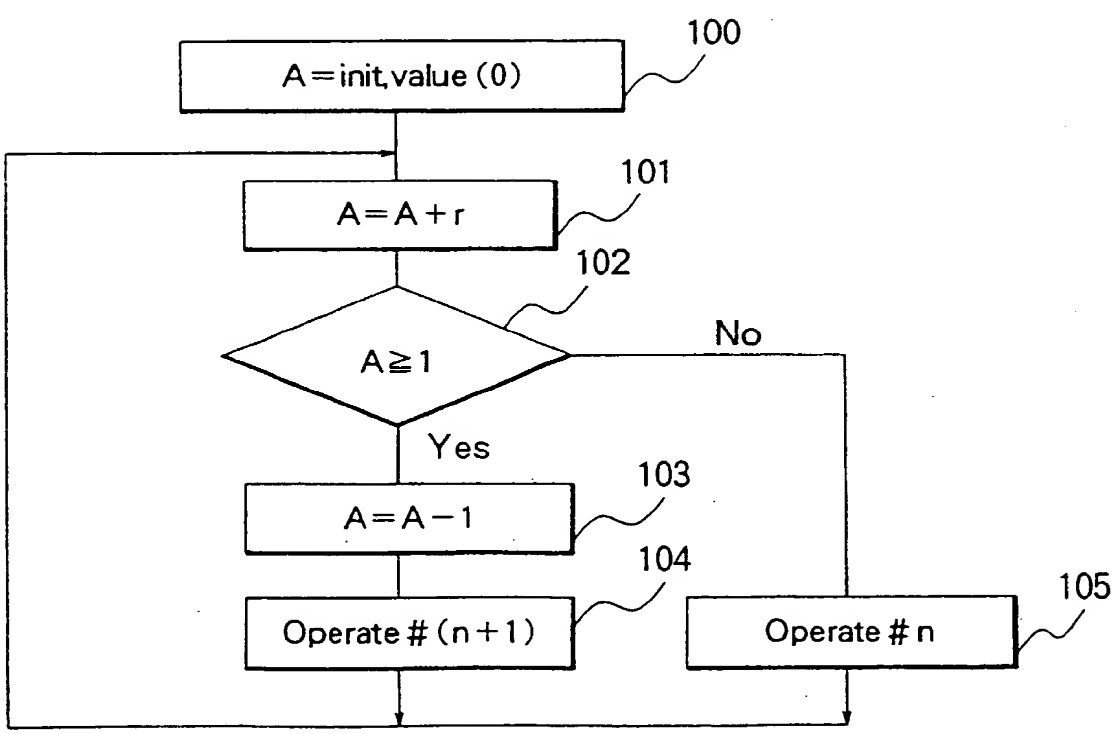

A=init.value (0)
100
A=A+r
101
102
A≧1
No
Yes
A=A−1
103
104
Operate # (n+1)
Operate # n
105

FIG. 16

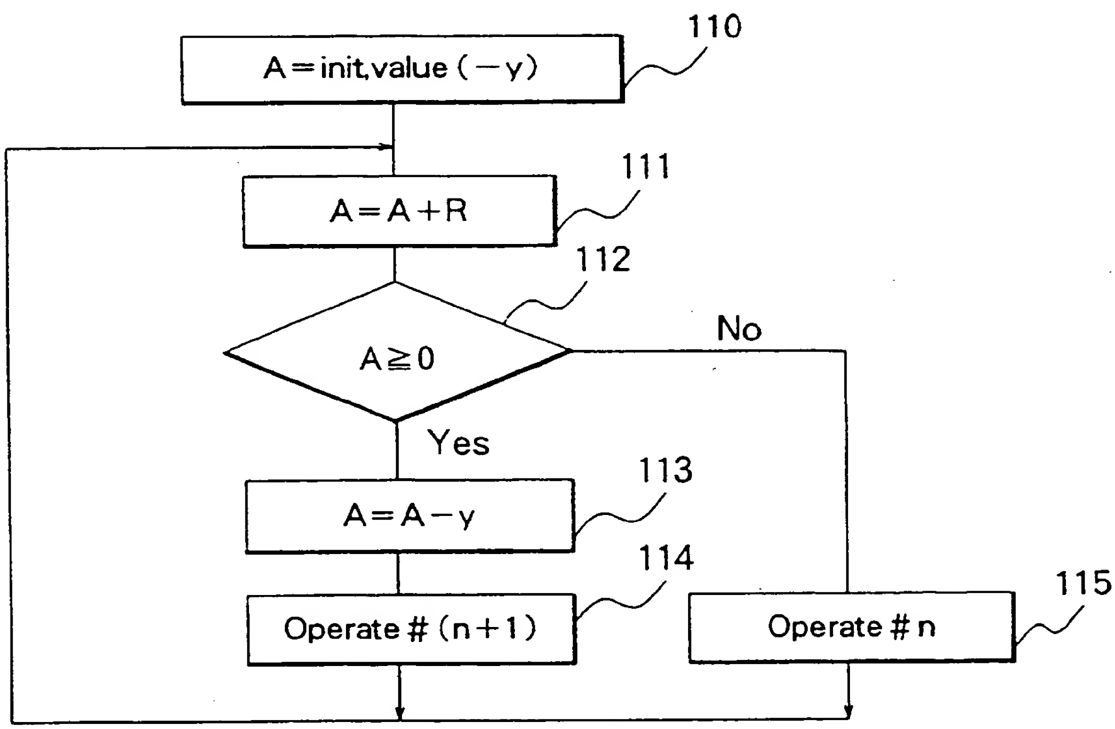
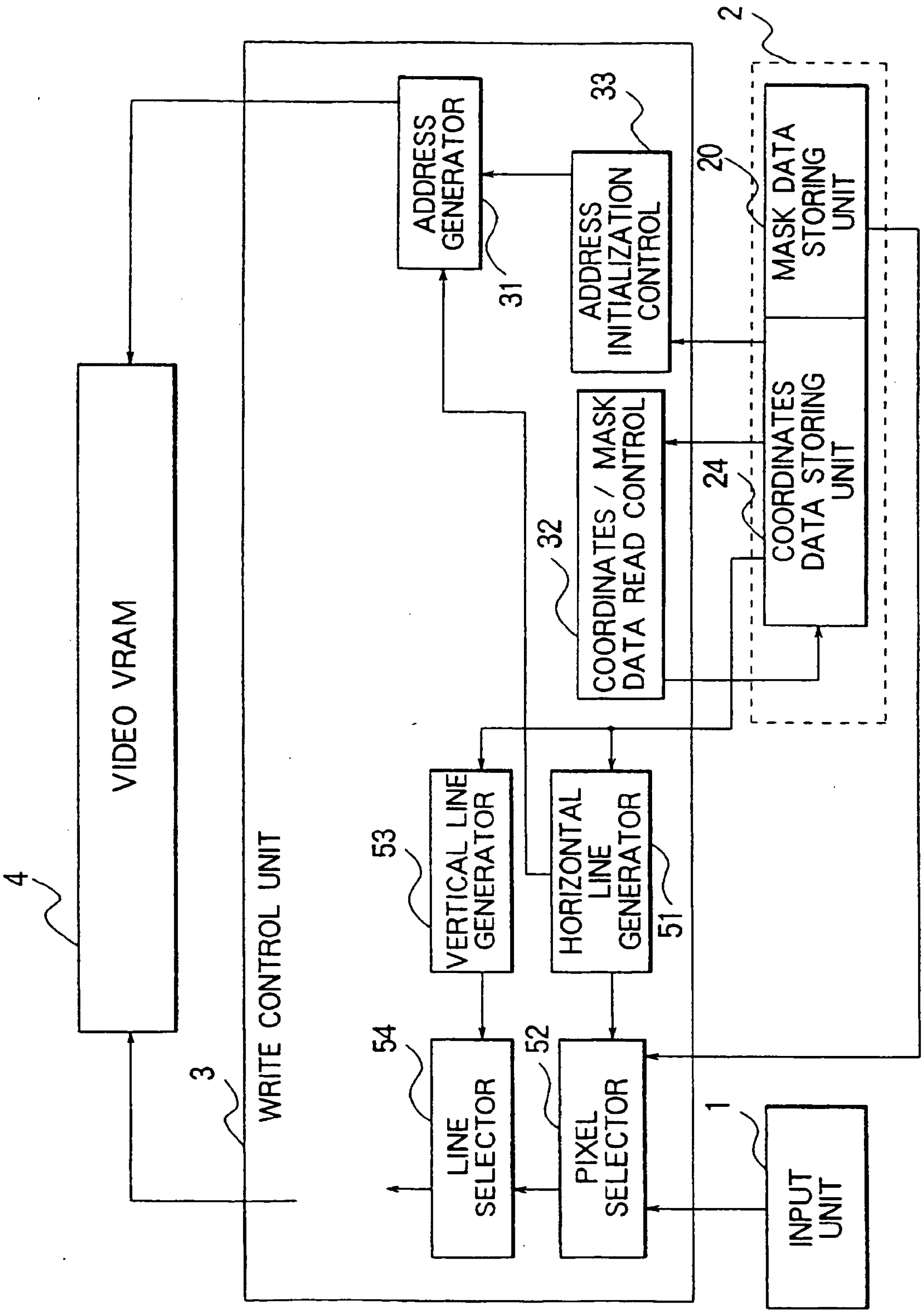

A = init.value (−y)
110
A = A + R
111
112
A≧0
No
Yes
A = A − y
113
114
Operate # (n + 1)
115
Operate # n

FIG. 17



VIDEO VRAM
WRITE CONTROL UNIT
ADDRESS GENERATOR
ADDRESS INITIALIZATION CONTROL
COORDINATES / MASK DATA READ CONTROL
MASK DATA STORING UNIT
COORDINATES DATA STORING UNIT
VERTICAL LINE GENERATOR
HORIZONTAL LINE GENERATOR
LINE SELECTOR
PIXEL SELECTOR
INPUT UNIT
1
2
3
4
20
24
31
32
33
51
52
53
54

FIG. 18

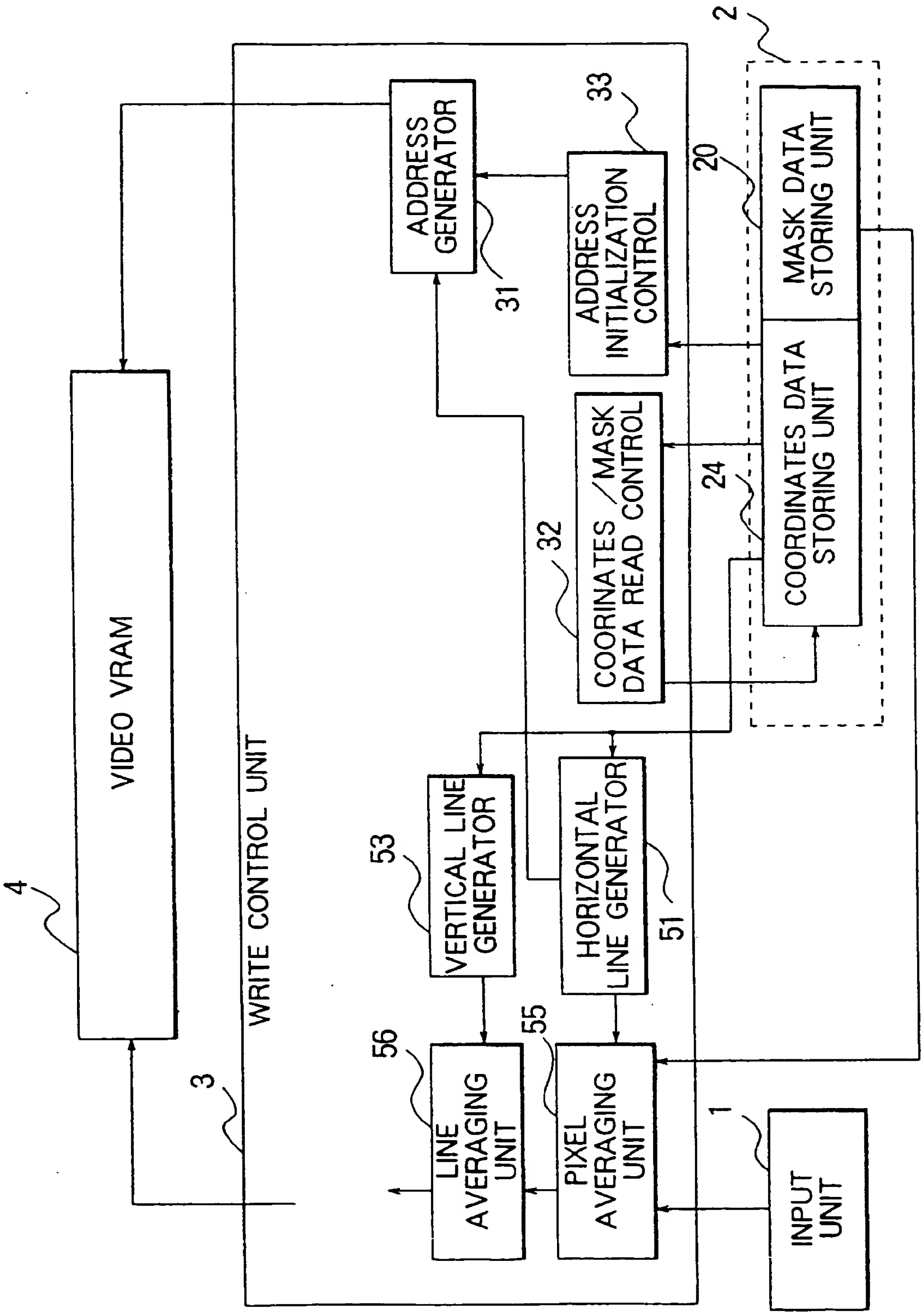

VIDEO VRAM
4
WRITE CONTROL UNIT
3
ADDRESS GENERATOR
31
ADDRESS INITIALIZATION CONTROL
33
COORINATES /MASK DATA READ CONTROL
32
VERTICAL LINE GENERATOR
53
HORIZONTAL LINE GENERATOR
51
LINE AVERAGING UNIT
56
PIXEL AVERAGING UNIT
55
MASK DATA STORING UNIT
20
COORDINATES DATA STORING UNIT
24
2
INPUT UNIT
1

FIG. 19

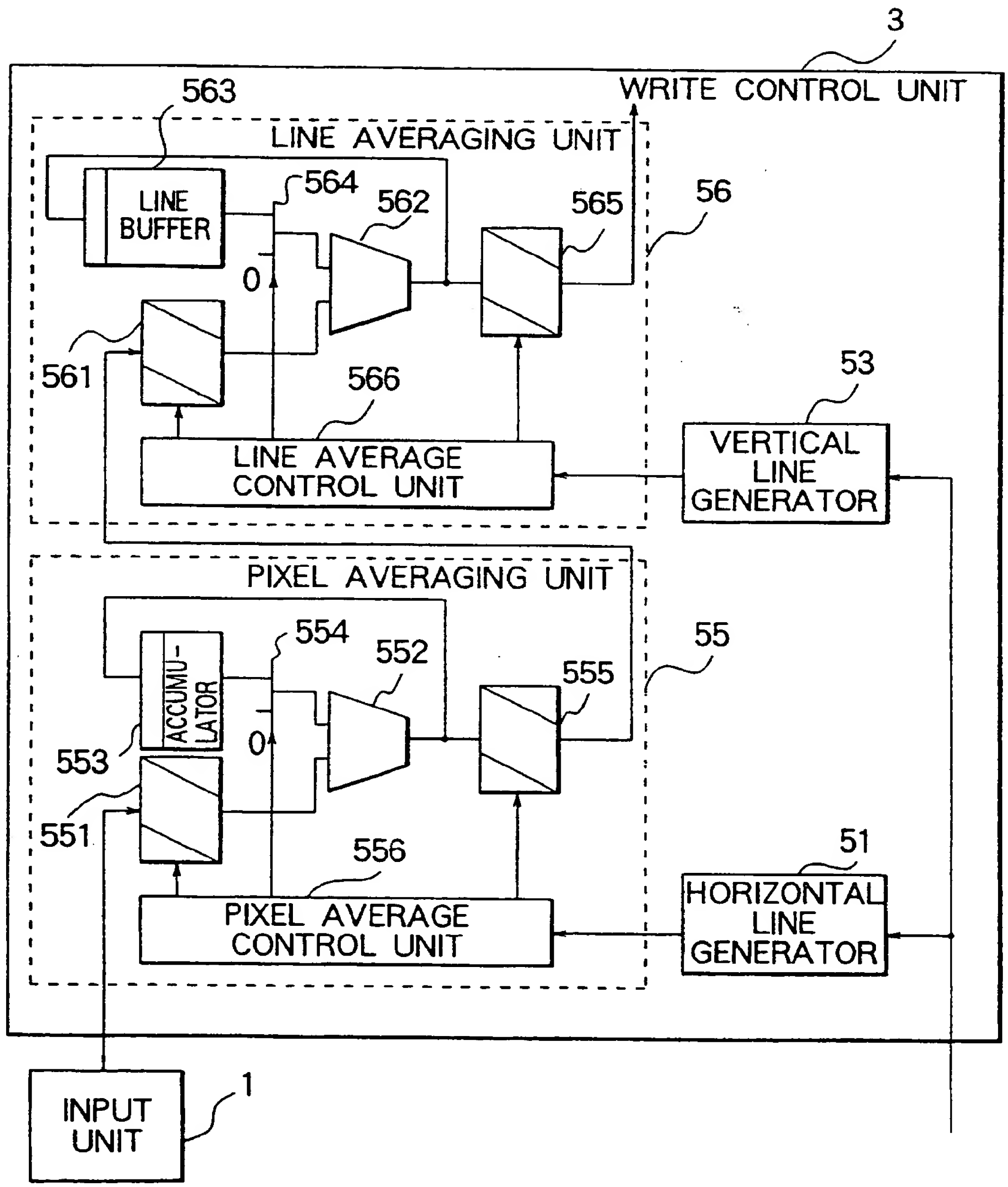

3
WRITE CONTROL UNIT
563
LINE AVERAGING UNIT
LINE BUFFER
564
562
565
56
0
561
566
53
LINE AVERAGE CONTROL UNIT
VERTICAL LINE GENERATOR
PIXEL AVERAGING UNIT
554
552
ACCUMU-LATOR
555
55
0
553
551
556
51
PIXEL AVERAGE CONTROL UNIT
HORIZONTAL LINE GENERATOR
INPUT UNIT
1

FIG. 20

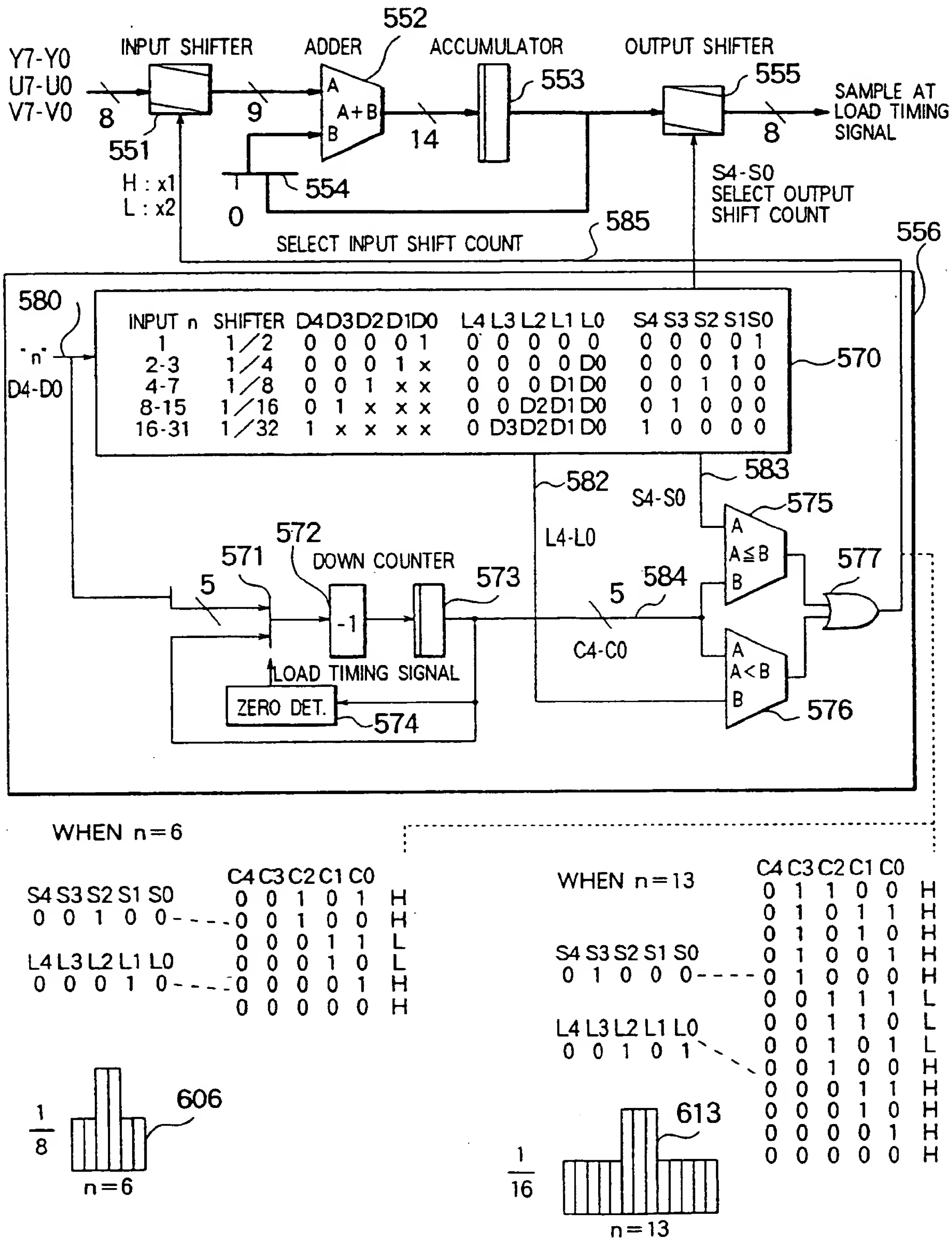

552
Y7-Y0
U7-U0
V7-V0
INPUT SHIFTER
ADDER
ACCUMULATOR
OUTPUT SHIFTER
553
555
SAMPLE AT LOAD TIMING SIGNAL
8
551
9
A
A+B
B
14
554
0
H : x1
L : x2
S4-S0 SELECT OUTPUT SHIFT COUNT
585
SELECT INPUT SHIFT COUNT
556
580
"n"
D4-D0
INPUT n SHIFTER D4 D3 D2 D1 D0 L4 L3 L2 L1 L0 S4 S3 S2 S1 S0
1 1/2 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1
2-3 1/4 0 0 0 1 x 0 0 0 0 D0 0 0 0 1 0
4-7 1/8 0 0 1 x x 0 0 0 D1 D0 0 0 1 0 0
8-15 1/16 0 1 x x x 0 0 D2 D1 D0 0 1 0 0 0
16-31 1/32 1 x x x x 0 D3 D2 D1 D0 1 0 0 0 0
570
582
583
S4-S0
575
L4-L0
A
A≤B
B
577
572
571
DOWN COUNTER
573
584
5
-1
C4-C0
A
A<B
B
LOAD TIMING SIGNAL
ZERO DET.
574
576
WHEN n=6
C4 C3 C2 C1 C0
S4 S3 S2 S1 S0
0 0 1 0 0
0 0 1 0 1 H
0 0 1 0 0 H
0 0 0 1 1 L
0 0 0 1 0 L
0 0 0 0 1 H
0 0 0 0 0 H
L4 L3 L2 L1 L0
0 0 0 1 0
WHEN n=13
C4 C3 C2 C1 C0
0 1 1 0 0 H
0 1 0 1 1 H
0 1 0 1 0 H
0 1 0 0 1 H
0 1 0 0 0 H
0 0 1 1 1 L
0 0 1 1 0 L
0 0 1 0 1 L
0 0 1 0 0 H
0 0 0 1 1 H
0 0 0 1 0 H
0 0 0 0 1 H
0 0 0 0 0 H
S4 S3 S2 S1 S0
0 1 0 0 0
L4 L3 L2 L1 L0
0 0 1 0 1
1/8
606
n=6
1/16
613
n=13

FIG. 21

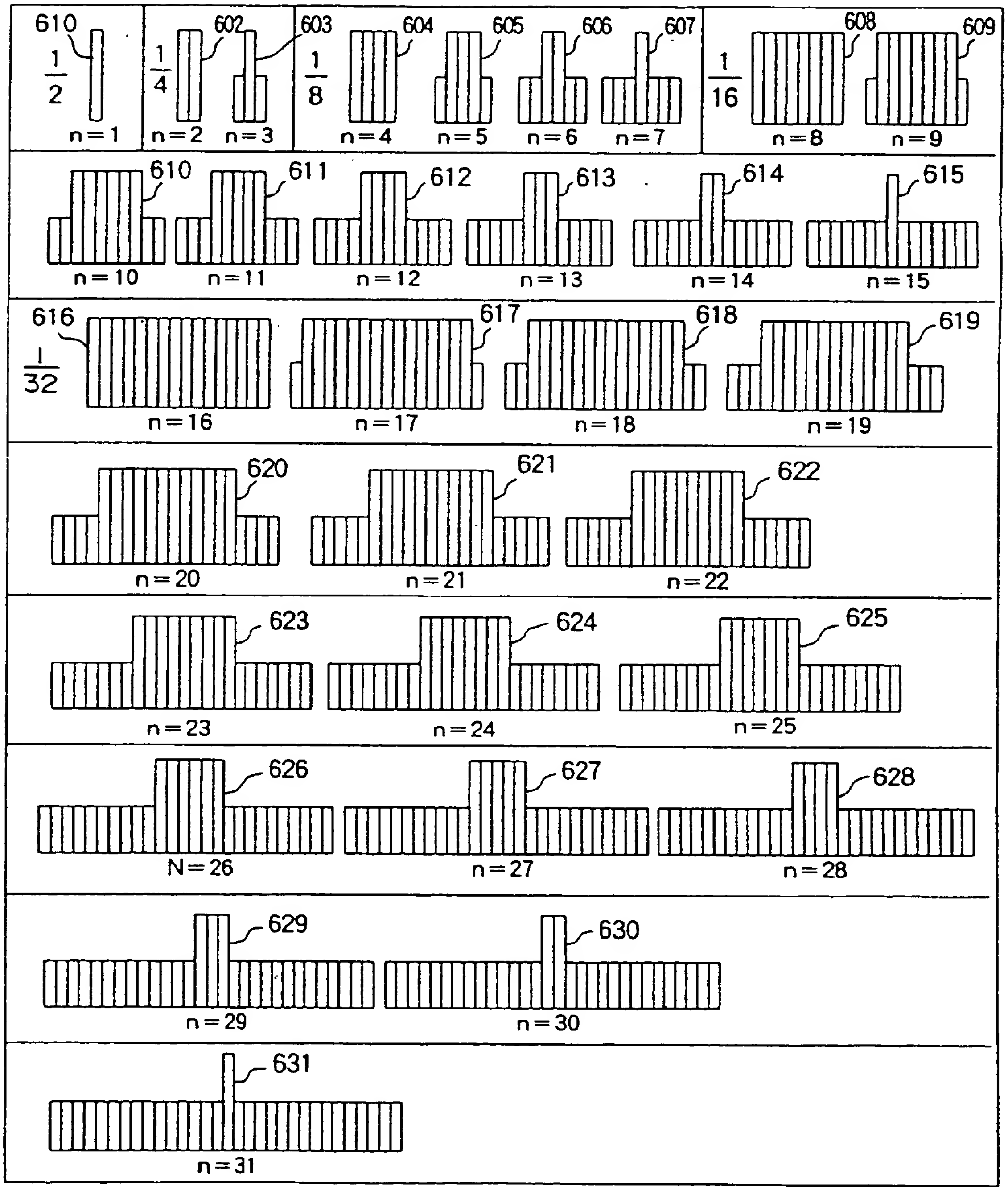
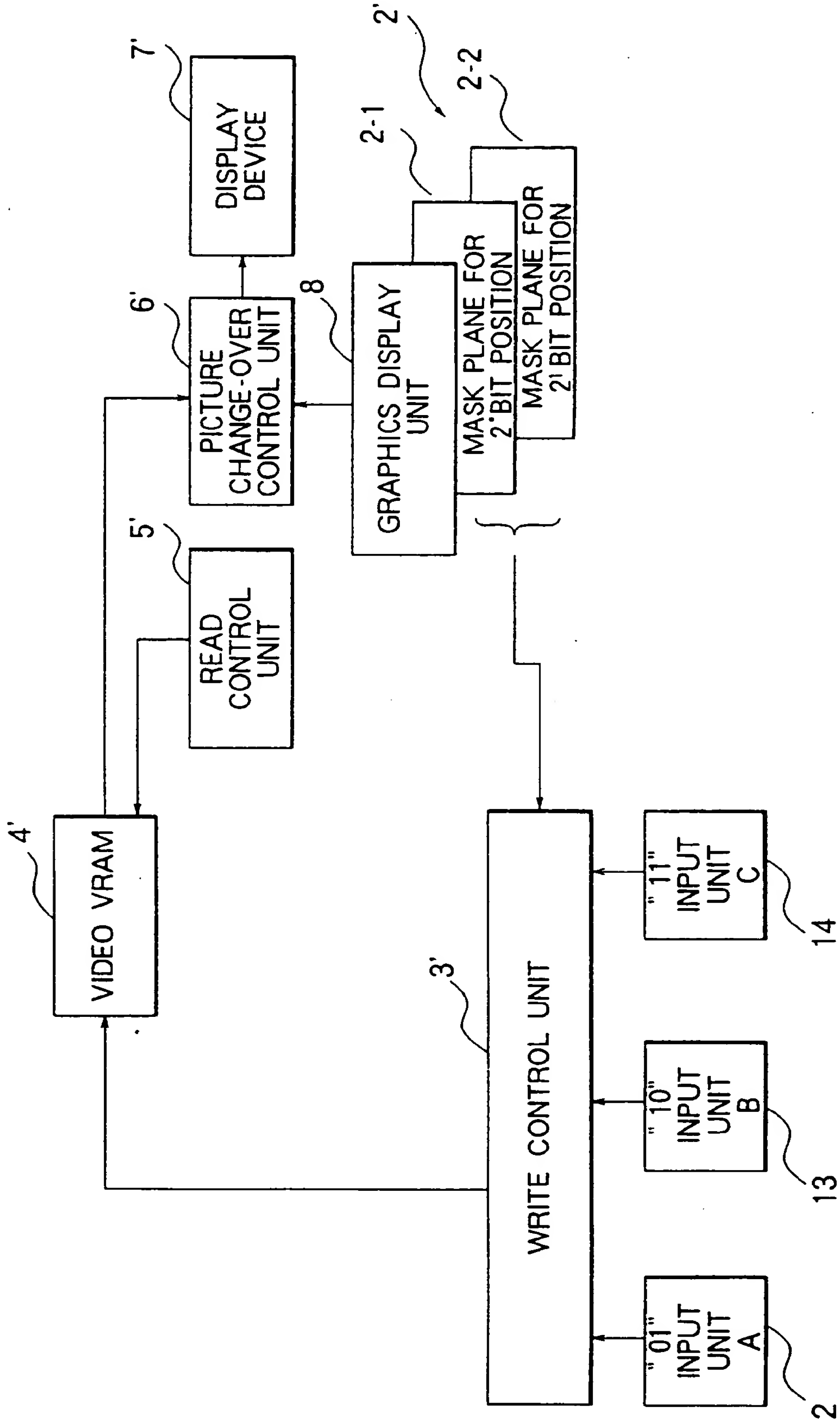

610
1/2
n=1
602
1/4
n=2
n=3
603
604
605
606
607
1/8
n=4
n=5
n=6
n=7
608
609
1/16
n=8
n=9
610
611
612
613
614
615
n=10
n=11
n=12
n=13
n=14
n=15
616
1/32
n=16
617
n=17
618
n=18
619
n=19
620
n=20
621
n=21
622
n=22
623
n=23
624
n=24
625
n=25
626
N=26
627
n=27
628
n=28
629
n=29
630
n=30
631
n=31

FIG. 22



DISPLAY DEVICE
7'
PICTURE CHANGE-OVER CONTROL UNIT
6'
READ CONTROL UNIT
5'
VIDEO VRAM
4'
GRAPHICS DISPLAY UNIT
8
MASK PLANE FOR 2'BIT POSITION
2-1
MASK PLANE FOR 2'BIT POSITION
2-2
2'
WRITE CONTROL UNIT
3'
"01" INPUT UNIT A
12
"10" INPUT UNIT B
13
"11" INPUT UNIT C
14

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 593 012 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
07.05.1997 Bulletin 1997/19

(43) Date of publication A2:
20.04.1994 Bulletin 1994/16

(21) Application number: 93116496.6

(22) Date of filing: 12.10.1993

(51) Int. Cl.[6]: G09G 1/16, G06F 3/14, G09G 5/14

(84) Designated Contracting States:
DE GB

(30) Priority: 13.10.1992 JP 274035/92

(71) Applicant: HITACHI, LTD.
Chiyoda-ku, Tokyo 100 (JP)

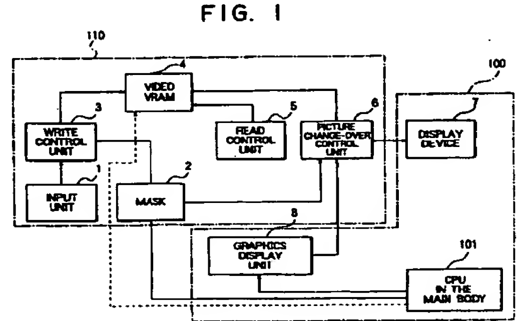
(72) Inventors:
- Kohiyama, Tomohisa
Totsuka-ku, Yokohama-shi (JP)
- Yamagishi, Masami
Zama-shi (JP)
- Yamada, Takahiro
Yokohama-shi (JP)
- Kamo, Munekazu
Hadano-shi (JP)
- Nomi, Makoto
Katsuta-shi (JP)
- Iwai, Noriyuki,
Hitachi Utsukushigaokaryo W232
Midori-ku, Yokohama-shi (JP)
- Minobe, Randy
San Jose, Ca 95124 (US)
- Jenney, Kim
San Jose, Ca 95126 (US)

(74) Representative: Altenburg, Udo, Dipl.-Phys. et al
Patent- und Rechtsanwälte,
Bardehle . Pagenberg . Dost . Altenburg .
Frohwitter . Geissler & Partner,
Galileiplatz 1
81679 München (DE)

(54) Video picture display device and method for controlling video picture display

(57) A video picture written in the bit map memory (4) is displayed in a redetermined area on the display screen (70) of the display device (7) within the computer main body (100). The masking memory (2) having a bit number equal to or less than the number of the pixels of the video picture to be inputted is provided separate from the bit map memory (4). When the pixel data of the video picture data has been inputted, the input pixel data is selectively written in the bit map memory (4) based on the contents of the masking memory (2). In displaying a compressed picture of the input video picture on the display screen, an oblique line generating algorithm is used.

FIG. 1



EP 0 593 012 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 11 6496

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X Y A	GB 2 215 956 A (BENCHMARK TECHNOLOGIES LTD.) * abstract * * page 16, line 10 - line 23 * * page 21, line 9 - page 22, line 5 * * page 51, line 3 - page 52, line 3 * * page 61, line 21 - page 62, line 16; figures 1-14 *	1,14 13 2-8, 15-18	G09G1/16 G06F3/14 G09G5/14
X Y A	US 4 947 257 A (FERNANDEZ ET AL) * abstract * * column 3, line 3 - line 25 * * column 2, line 57 - line 61 *	18 13 6-8,16, 17	
A	EP 0 431 845 A (RASTEROPS CORP.) * abstract * * page 3, line 4 - line 13 * * page 7, line 1 - line 13 * * page 7, line 40 - page 8, line 6 *	1-8, 13-18	TECHNICAL FIELDS SEARCHED (Int.Cl.5) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 November 1996	D.J. O'REILLY

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)